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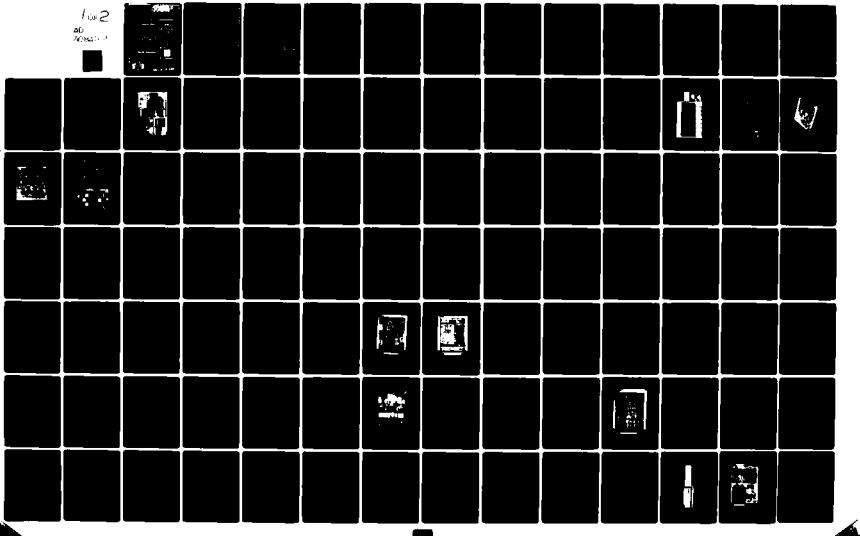

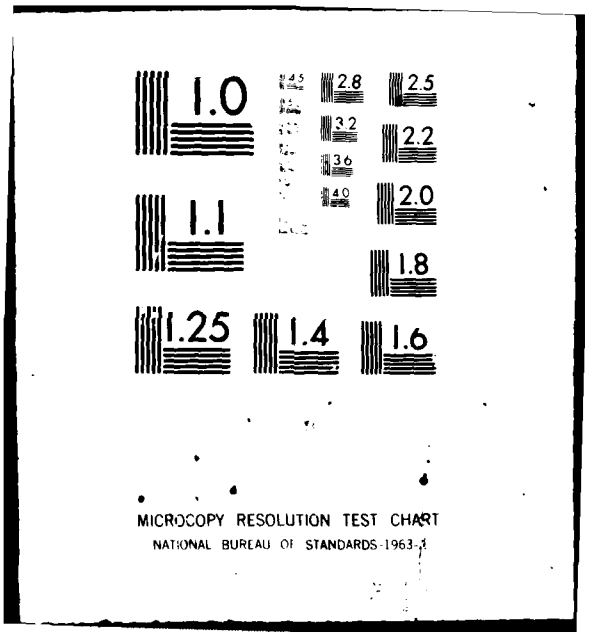
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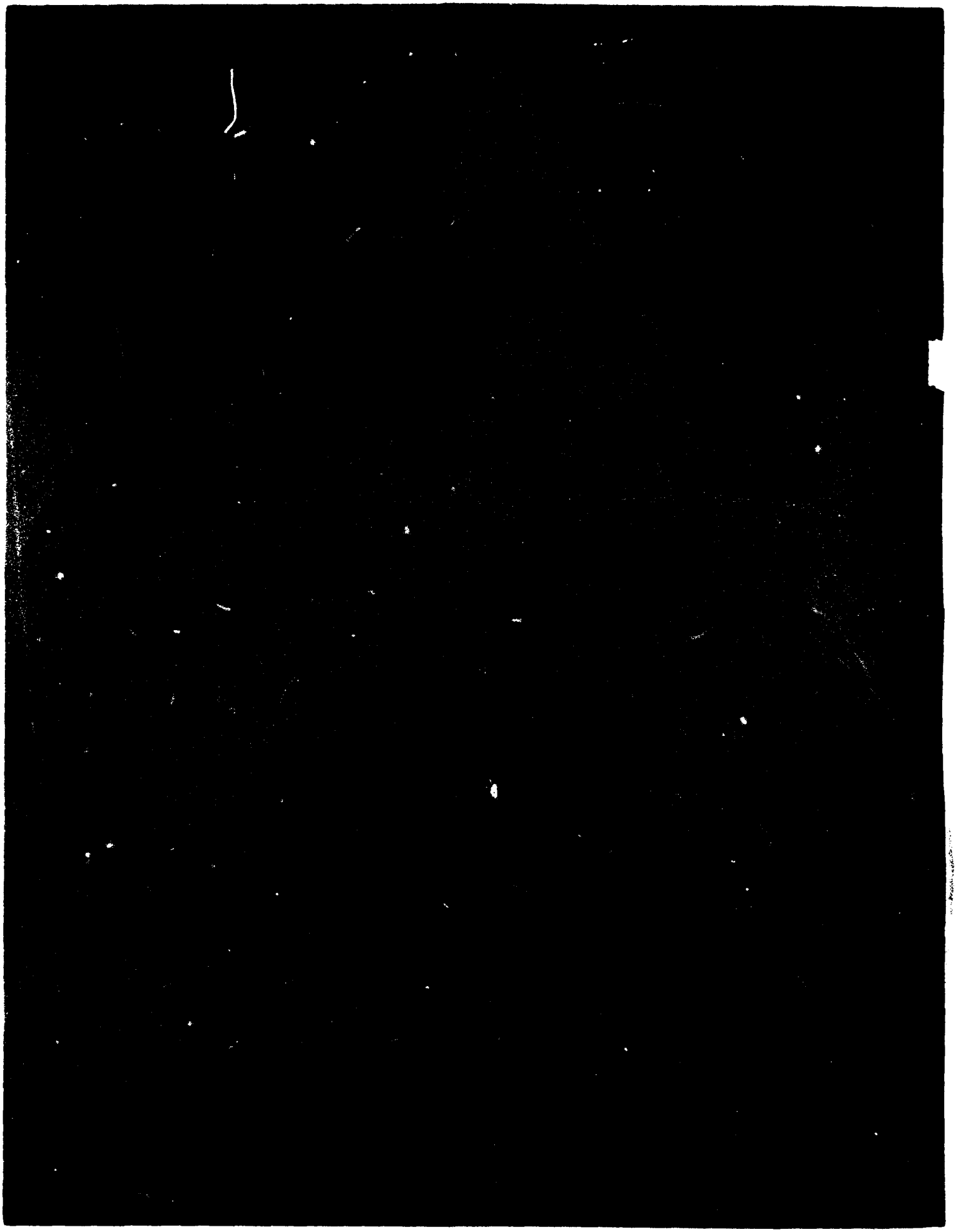

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

FEEDBACK NULLING DEMONSTRATION SYSTEM HARDWARE

D. A. SIEGEL
D. M. HODSDON
B. M. POTTS
H. S. BABBITT
E. S. DAVIS
W. K. HUTCHINSON
K. LEEDS

Division 6

TECHNICAL NOTE 1979-12

23 NOVEMBER 1979

LEXINGTON MASSACHUSETTS

ABSTRACT

The Lincoln Laboratory analog-feedback adaptive antenna nulling demonstration system hardware is described with discussion of design theory, implementation, problems, and trade-offs encountered. System and subsystem block diagrams and photos of actual hardware are included. Peripheral test equipment is discussed along with built-in telemetry and recording capabilities.

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I. OVERVIEW

As part of the technology development of anti-jam satellite communications, Lincoln Laboratory has developed, built, and tested a demonstration analog-feedback adaptive-nulling antenna system. The system, which is based on the Howells-Applebaum feedback loop, is designed to increase the signal-to-interference ratio when desired signals operate in the presence of interference signals. The signals received from interfering or undesirable signal sources are minimized by appropriately modifying the antenna radiation pattern so as to attenuate signals from the direction of those sources relative to the desired signals. The demonstration system consists of a simulated array of antenna elements and uplink signals and a real-time adaptive receiver-processor which controls the weighting of each element signal prior to combining. The weighting process involves changing the relative amplitudes and phases of the received signals thus changing the effective receiving radiation pattern of the antenna, i.e., its relative response to signals arriving from different directions.

The system operation involves taking the signals from N independent antenna elements and weighting and combining them to form a single output signal in which the signal-to-interference ratio is enhanced over what it is for any individual antenna element. The task of the nulling processor is to select the set of weights for the antenna element array in some optimum fashion. The feedback processor implemented determines the weights by sensing the correlation between the combined output and the output of each individual antenna element. The correlator output for each element is then used to control the weight setting for that particular element. The weight settings, expressed as a vector, eventually adapt to a steady-state value $\underline{W} \approx [\underline{\underline{I}}+\mu\underline{\underline{R}}]^{-1} \cdot \underline{V}$. $\underline{V}$ is the initial, unadapted, set of weights that is selected to give an Earth-coverage antenna-gain pattern in the absence of interference signals, $\underline{\underline{R}}$ is the $N \times N$ covariance matrix of the antenna element received signals, $\underline{\underline{I}}$ is the identity matrix, and μ is a variable threshold loop gain. Additional theoretical background information is contained in Refs. 1 through 6. It is the purpose

of this Technical Note to describe the hardware used to implement the Lincoln Laboratory analog-feedback adaptive-nulling antenna system demonstration.

The performance goals for the system were:

Nulling bandwidth	10 MHz
Signal bandwidth	1 MHz
Dynamic range of jammers to be nulled	40 dB
Loop adaptive time constant	10 μsec to 13 msec
Processor cancellation over 0-10 MHz band	$\geq$ 40 dB

In most respects, these goals have been met and/or exceeded. Lincoln Laboratory Technical Notes TN 1979-13, 14, and 15 (Refs. 7 through 9) present the results of the system testing and discuss system performance.

Figure 1.1 shows a block diagram of the hardware developed for the demonstration system. The boxes in the center portion of the figure comprise the adaptive processor. The remaining boxes are largely support and test items. The specific sections to be covered in this report include the RF front-end, the weight and summer networks, the correlation and control units, the digital logic (hardware and software), the A/D — D/A interface circuits, and system control, telemetry, and instrumentation. Table 1.1 lists all the Lincoln Laboratory Technical Notes associated with the analog-feedback adaptive nulling antenna system.

The RF front-end provides preamplification of the received signal which is desirable to insure that attenuation by ensuing operations (frequency translation and weighting) does not degrade the system signal-to-noise (S/N) ratio. Frequency translation is desirable for reducing coupling between antenna elements and the output of the summer network and to allow weight, combiner, and filter circuits to be implemented at a convenient IF frequency. Appropriate filters are used to limit signals to that band of the frequency spectrum over which effective nulling can be realized. As previously mentioned, the weight and summer network changes the relative amplitude and phase of the received signals and sums the results. The weighting is done in accordance

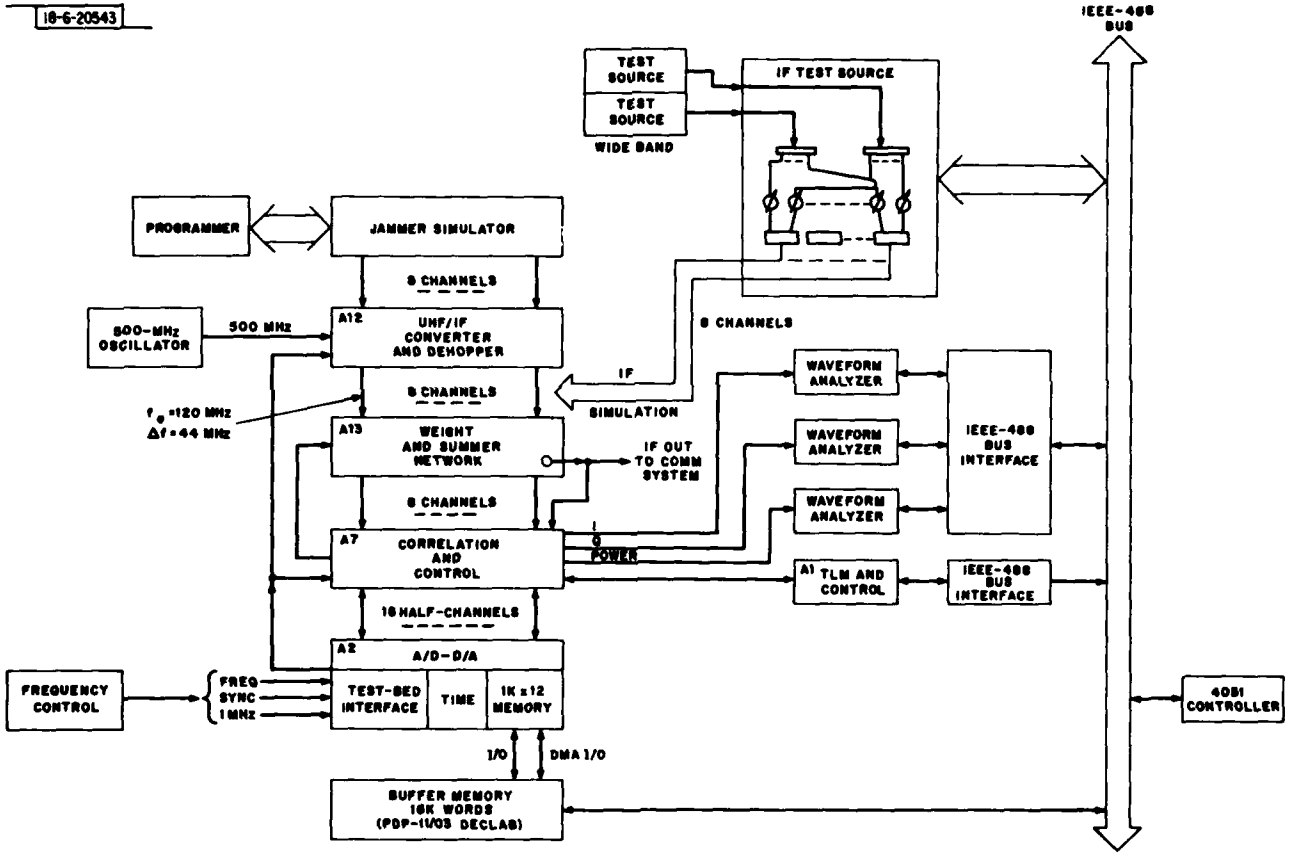

Fig. 1.1. Block diagram of the analog-feedback adaptive-nulling processor demonstration system.

TABLE 1.1

LINCOLN LABORATORY TECHNICAL NOTES

ASSOCIATED WITH THE

ANALOG-FEEDBACK ADAPTIVE NULLING ANTENNA SYSTEM

TN 1979-8	A UHF Simulator for Antenna Nulling System, W. C. Cummings, T. P. Robbio, W. C. Provencher, J. E. Drover, and M. Singhal
TN 1979-9	RF Front-ends for Feedback Nuller, D. M. Hodsdon
TN 1979-10	PIN Diode Weight Circuits, B. M. Potts
TN 1979-11	Transconductance Multipliers for Weight Circuits in an Adaptive Nulling System, J. N. Wright
TN 1979-12	Feedback Nulling Demonstration System Hardware, D. A. Siegel, D. M. Hodsdon, B. M. Potts, H. S. Babbitt, E. S. Davis, W. K. Hutchinson, and K. Leeds
TN 1979-13	Feedback Processor Test Results, J. T. Mayhan, F. W. Floyd, and D. A. Siegel
TN 1979-14	Factors Affecting the Performance of Adaptive Antenna Systems and Some Evaluation Techniques, J. T. Mayhan, and F. W. Floyd
TN 1979-15	Some Effects of Hard Limiting in Adaptive Antenna Systems, F. W. Floyd and J. T. Mayhan

with the correlation and control unit which correlates the combined signal output with the output from each individual element. The A/D – D/A circuits interface the analog and digital portions of the system. Beam steering information (which defines the desired receive beam in the absence of interference) and weight information (which defines the adapted receive beam with nulls) are stored, transferred, and updated by the digital section. The digital section, in conjunction with the other support and test equipment, provides the necessary timing and coordination of events.

Figure 1.2 is a photograph of the Lincoln Laboratory analog-feedback adaptive-nulling system with associated controllers, computers, and some test hardware. As configured, the system is for technical demonstration purposes only; an actual flight system would have to be significantly smaller in physical size and weight and consume less power. Studies indicate that a flight system would be on the order of 40 pounds and consume 28 watts of power (including a 7-element double triangle antenna array).

Figure 1.3 is a more detailed block diagram of the analog-feedback adaptive-nulling system and will be referred to throughout this document.

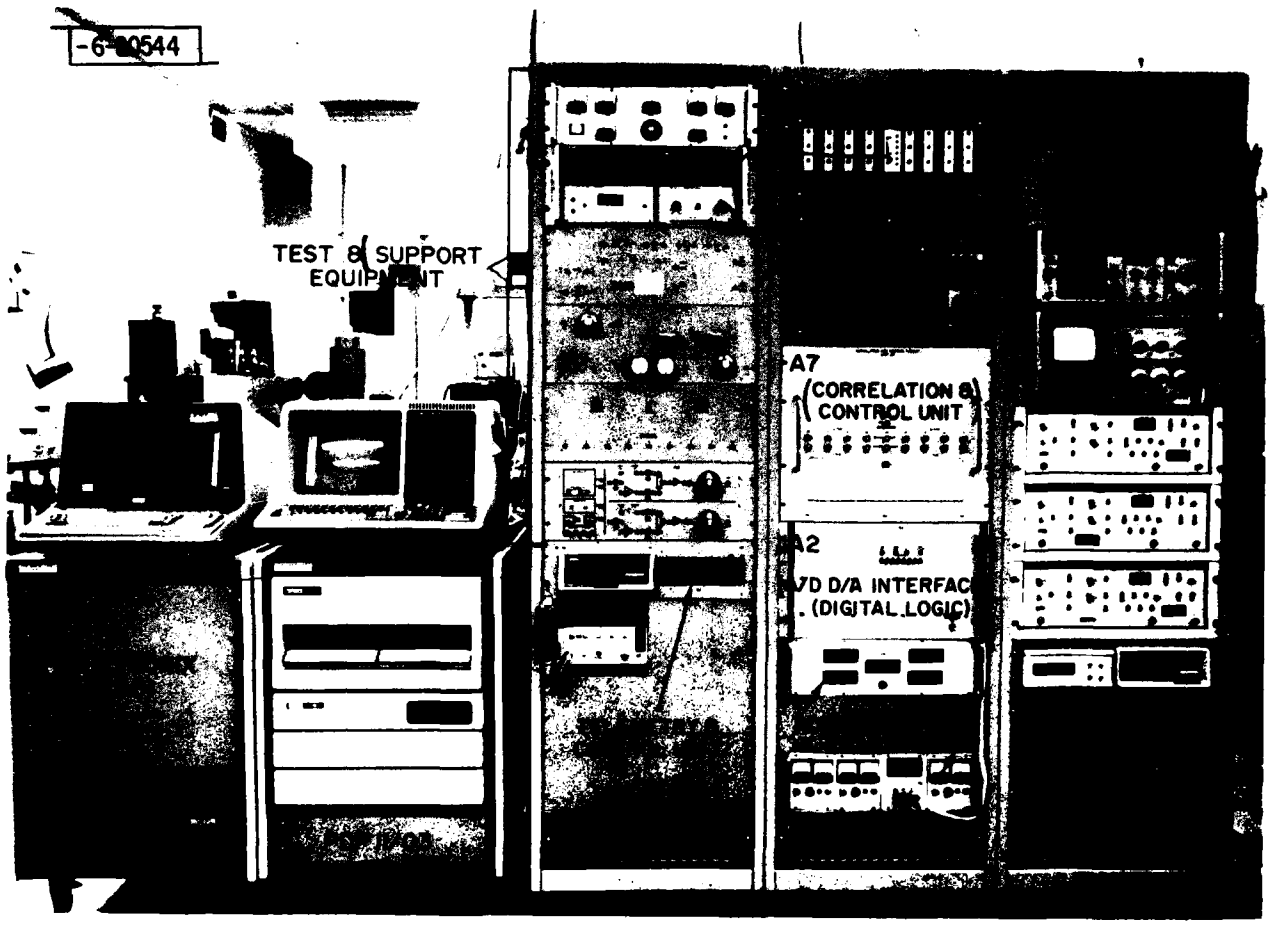

Fig. 1.2. Analog-feedback adaptive-nulling antenna demonstration system.

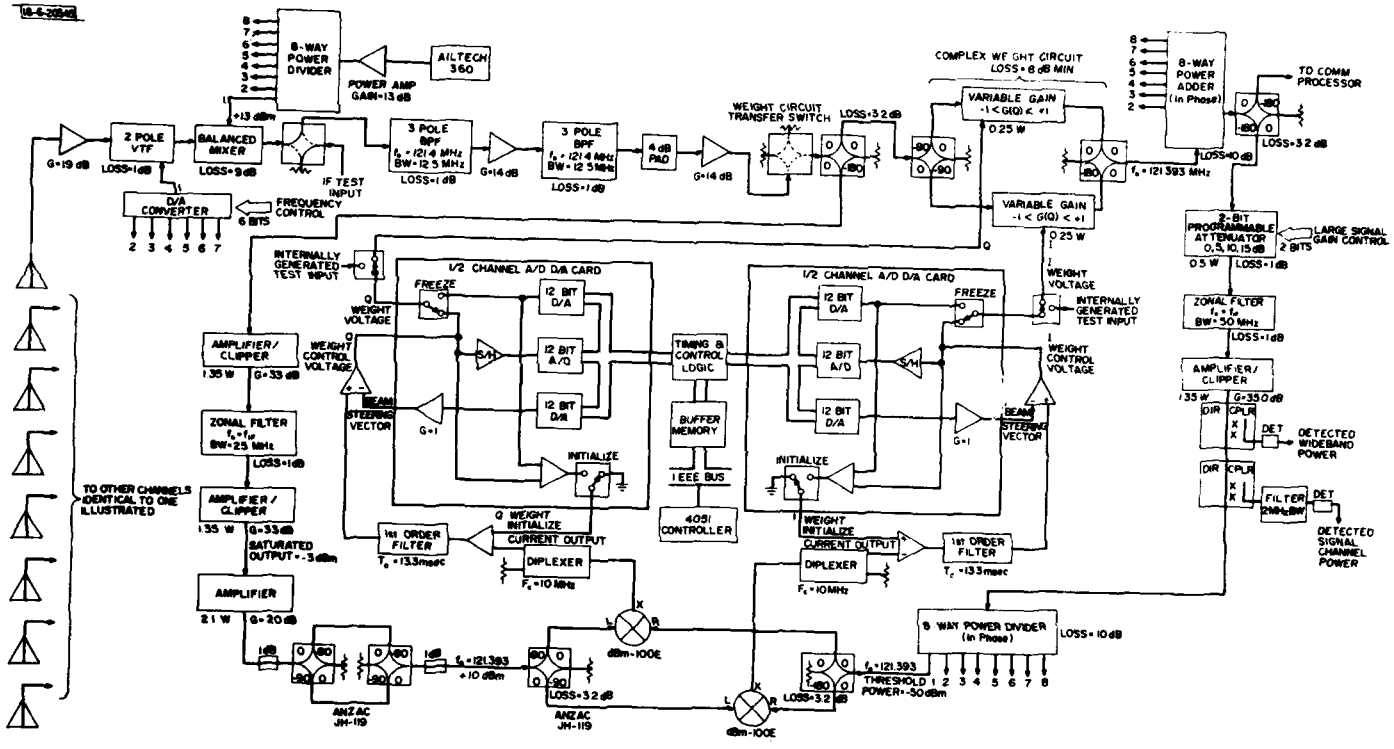

Fig. 1.3. Feedback nulling demonstration system block diagram.

II. UHF FRONT-END

The nulling front-end consists of 9 modules. There are 8 matched, single conversion, superheterodyne receivers, and one local oscillator drive conditioner. Each receiver of the front-end, Fig. 2.1, is preceded by RF preamplification to overcome mixer losses and to establish system noise figure. The preamplifier is followed by a 2-pole narrow-band voltage-tuned filter which tracks the receiver local oscillator. It has a bandwidth about twice that of the overall receiver bandwidth. Each filter is controlled by a common tuning voltage generated in the local oscillator drive conditioner.

The voltage-tuned filter is followed by a single-sideband mixer which converts the incoming RF signal to the system intermediate frequency. A single-sideband mixer was selected to provide image rejection in order to maintain the preselector complexity at a minimum, and to provide isolation between the first IF filter and the voltage-tuned preselector. The mixer provides greater than 30 dB image rejection and has about 40 dB of reverse isolation.

The overall receiver selectivity is set by two 3-pole bandpass filters separated by isolation amplifiers. The amplifiers use a cascode circuit to provide better than 50 dB of reverse isolation. A transfer relay is provided after the mixer to facilitate intermediate frequency testing.

Three major considerations were used to obtain the channel match required for adequate system performance. The first was to use components whose input and output VSWR were less than 1.2 over the frequencies of interest. This insured that interface mismatches did not introduce additional amplitude and phase ripple in the front-end transfer characteristic after assembly. The second consideration was to isolate all filters from each other by at least 40 dB. This guaranteed that multiple reflections through the filters did not add random amplitude and phase ripple. The third consideration was to match all critical parts such as capacitors and inductors in the filters and amplifiers before construction of the component.

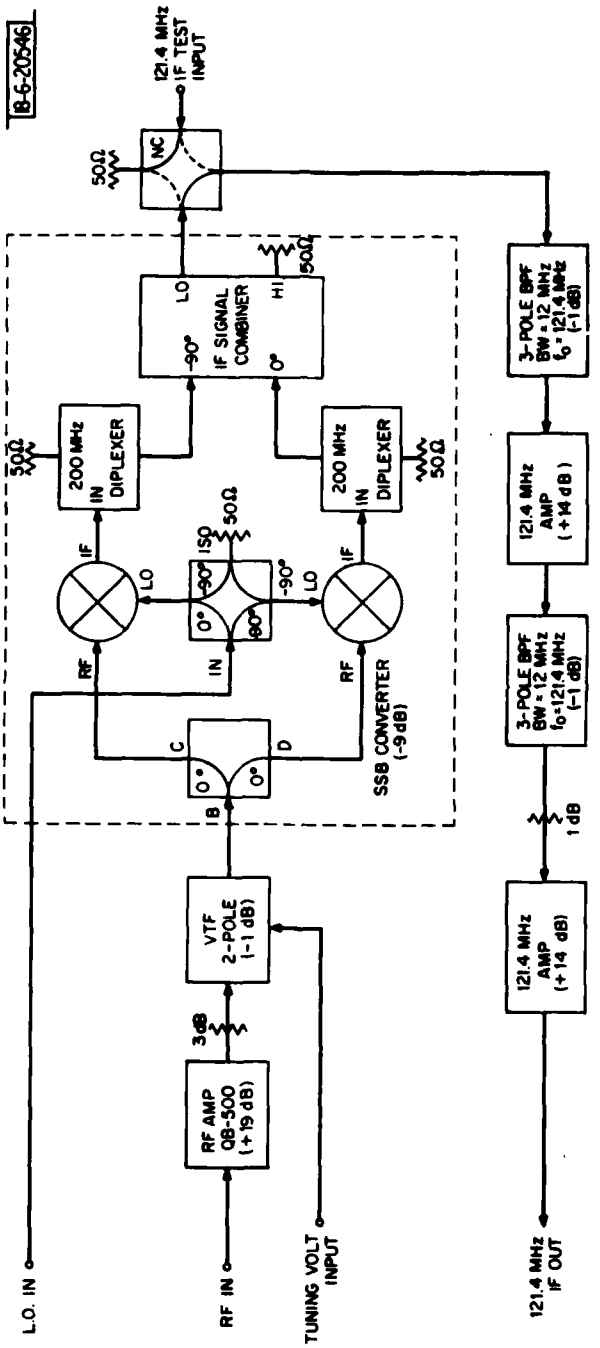

Fig. 2.1. UHF converter module.

The alignment technique used for the front-ends was to first align each component for a response as close to the expected theoretical characteristic as possible, and then trim the alignment until all corresponding components for the 8 channels were matched. The front-ends were then assembled and checked for match. Some additional minor adjustment of the IF filters and the voltage-tuned preselectors was made to maintain the match obtained at the component level.

The local oscillator drive conditioner, Fig. 2.2, takes the output of a synthesizer and conditions it for use as a common local oscillator for each of the 8 receiver channels. The conditioning consists simply of amplification and filtering to eliminate harmonics, followed by an 8-way power split using a phase-matched power divider. The diplexer before the 8-way power divider is required to provide a low VSWR termination at the intermediate frequency. This is necessary to minimize coupling between channels via the local oscillator line. A power monitor is provided to give a continuous indication of the local oscillator drive level.

A common tuning voltage is generated for the front-end voltage-tuned filters from a 6-bit frequency control word. The digital input is first translated by a read-only-memory, and then D/A converted to provide the required tuning voltage for a given input frequency. The read-only-memory is required because the voltage-tuned filters use varactors as the tuning element which results in a non-linear voltage vs center frequency characteristic.

The UHF front-ends are described in greater detail in Technical Note 1979-9 (Table 1.1).

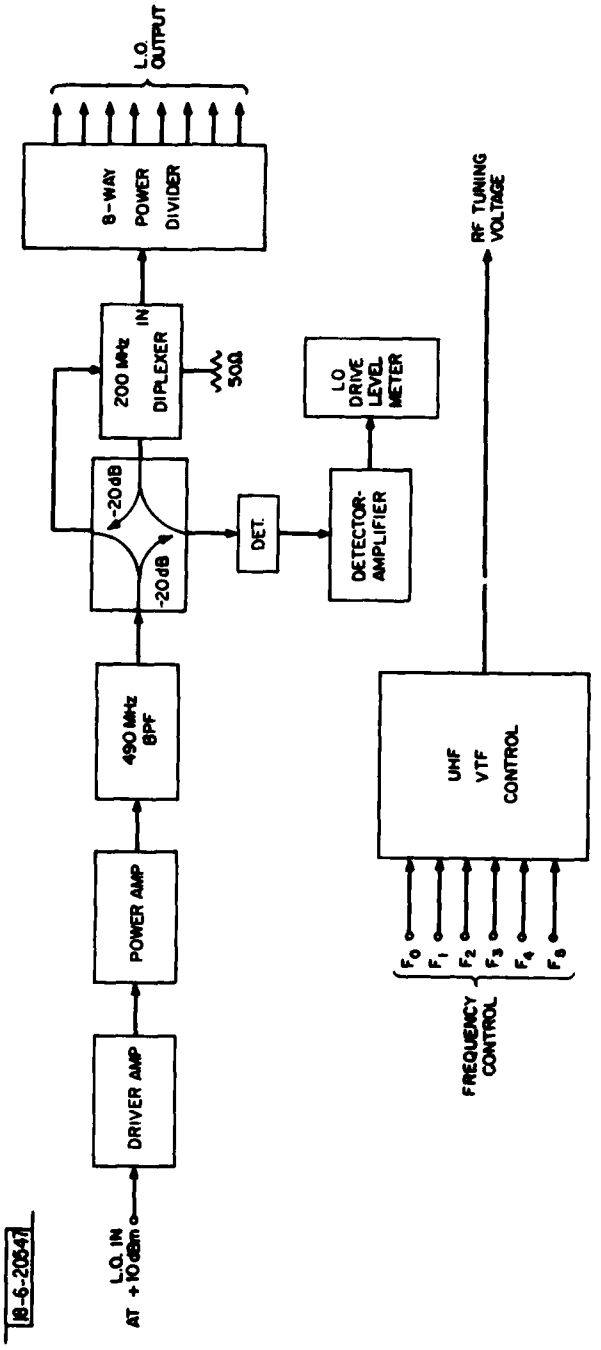

Fig. 2.2. UHF LO drive conditioner.

III. WEIGHT AND SUMMER NETWORK

3.1 Introduction

The Weight and Summer Network (WSN), identified as A13 in the system interconnection diagram of Fig. 3.1, consists of the following three major subsystems:

a. Weight Modules

b. Combiner Network

c. Telemetry, Control and Monitor Network

A simplified block diagram of the Weight and Summer Network is shown in Fig. 3.1. With the processor operating in its closed-loop feedback mode, input signals from the UHF/IF Converter unit (A12, Section II) are applied to each channel through a transfer switch. Depending upon the position of the switch, the input signal is either connected to a load in which case the channel is inoperative, or connected through the switch to the two-way power divider. In this manner, the transfer switch provides the flexibility of connecting from one to all of the signal channels, thereby allowing the processor to operate with varying numbers of channels. The two-way power divider at the output of the transfer switch separates the input signal into two paths, with one signal path being connected to the input of the weight circuit and the other to the Correlation and Control unit (A7). The latter signal, when correlated with the signal at the processor output, generates (in A7) the weight control voltages, V_I and V_Q, which are applied through a pair of single-pole-double-throw (SPDT) switches to the weight driver circuit. The driver circuit, in turn, generates the appropriate bias signals for setting the weight circuit attenuators.

The processor can also be operated in a manual or non-feedback mode for test purposes by disconnecting the weight control voltages from the Correlation and Control unit using the SPDT switches, and using control voltages generated by a reference circuit within A13. This mode of operation is particularly useful for troubleshooting individual channels of the processor. It also allows the operating condition of the weight circuits to be observed via the telemetry link or by the weight monitor circuit within A13.

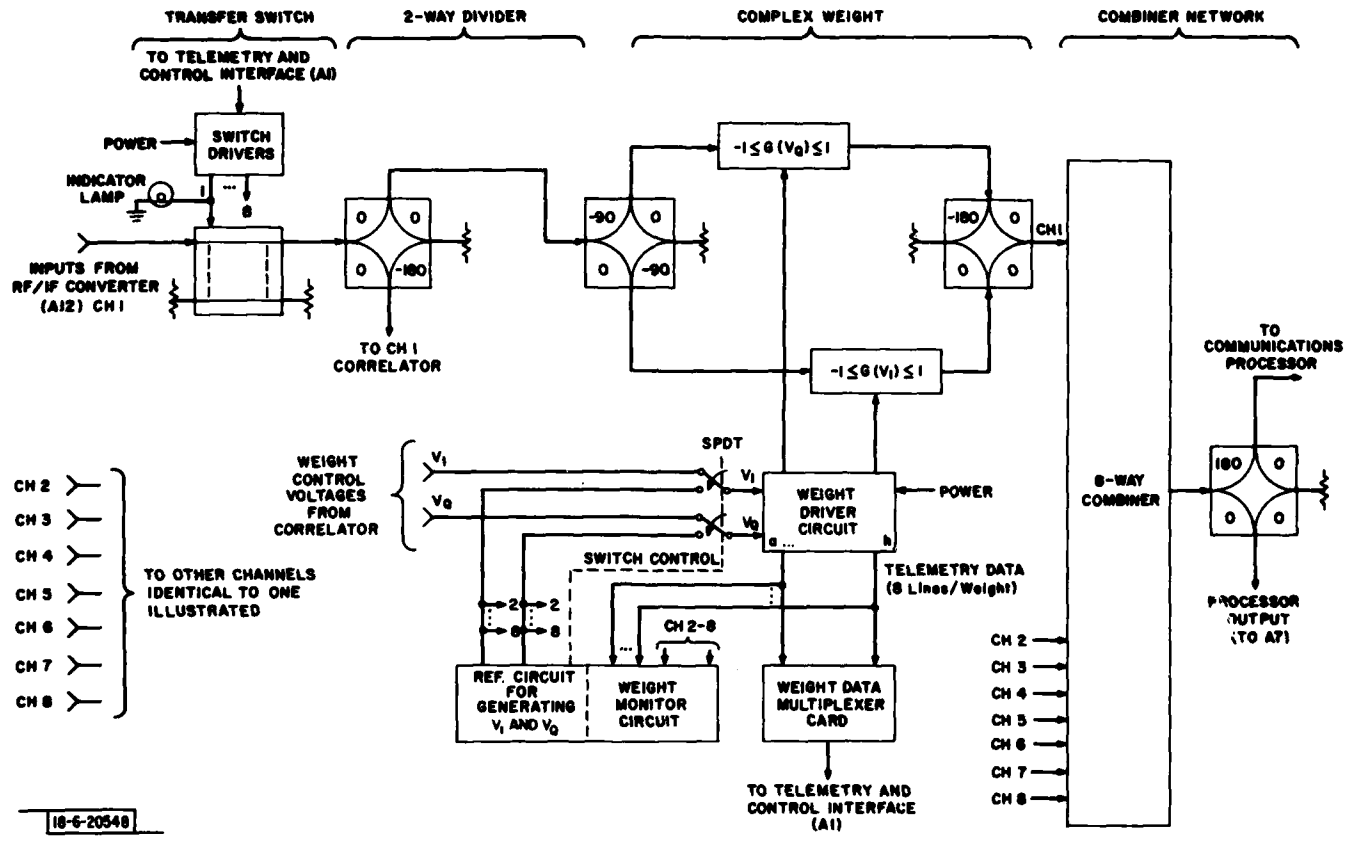

Fig. 3.1. Weight and combiner network block diagram.

Figure 3.2 shows a front view of the completed WSN assembly with the left-front cover removed. The WSN assembly is partitioned into two parts with the left-hand side containing the weight modules, the combiner network, the SPDT control voltage switches and various interconnecting cables. The right-hand side contains the telemetry, control, and weight monitor circuits. Shown on the top right-hand side front panel are eight indicator lamps which are used to monitor the status of the transfer switches. Below that is an LED panel meter which is used for setting the V_I and V_Q control voltages from the reference circuit, and for displaying the weight telemetry data. A rear view of the WSN assembly, in Fig. 3.3, shows the transfer switches and the various input-output connections.

3.2 Subsystem Description

3.2.1 Weight Modules

Three sets of weight modules were fabricated and installed in the Weight and Summer Network during the process of testing the adaptive processor. The design, fabrication and performance of these various weight designs have been described in detail in previous reports (Refs. 10 and 11). The three weight circuits are listed below in the order in which they were tested in the WSN assembly, and are shown in Figs. 3.4, 3.5 and 3.6.

1. Narrowband PIN Diode Weight
2. Transconductance Multiplier Weight
3. Broadband PIN Diode Weight

All weight modules were designed to be mechanically and electrically compatible to facilitate their installation and removal from the Weight and Summer Network. The first two sets of weights (Figs. 3.4 and 3.5) were fabricated individually in modules measuring 5.50 × 5.50 × 1.625 inches. Each module contains the two-way power divider preceding the weight (see Fig. 3.1), the weight circuit and its associated driver circuit. The construction of the broadband PIN diode weight modules (Fig. 3.6) was slightly

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Fig. 3.2. Front-view of the weight and combiner network assembly (A13) with left-front cover removed to show weight modules.

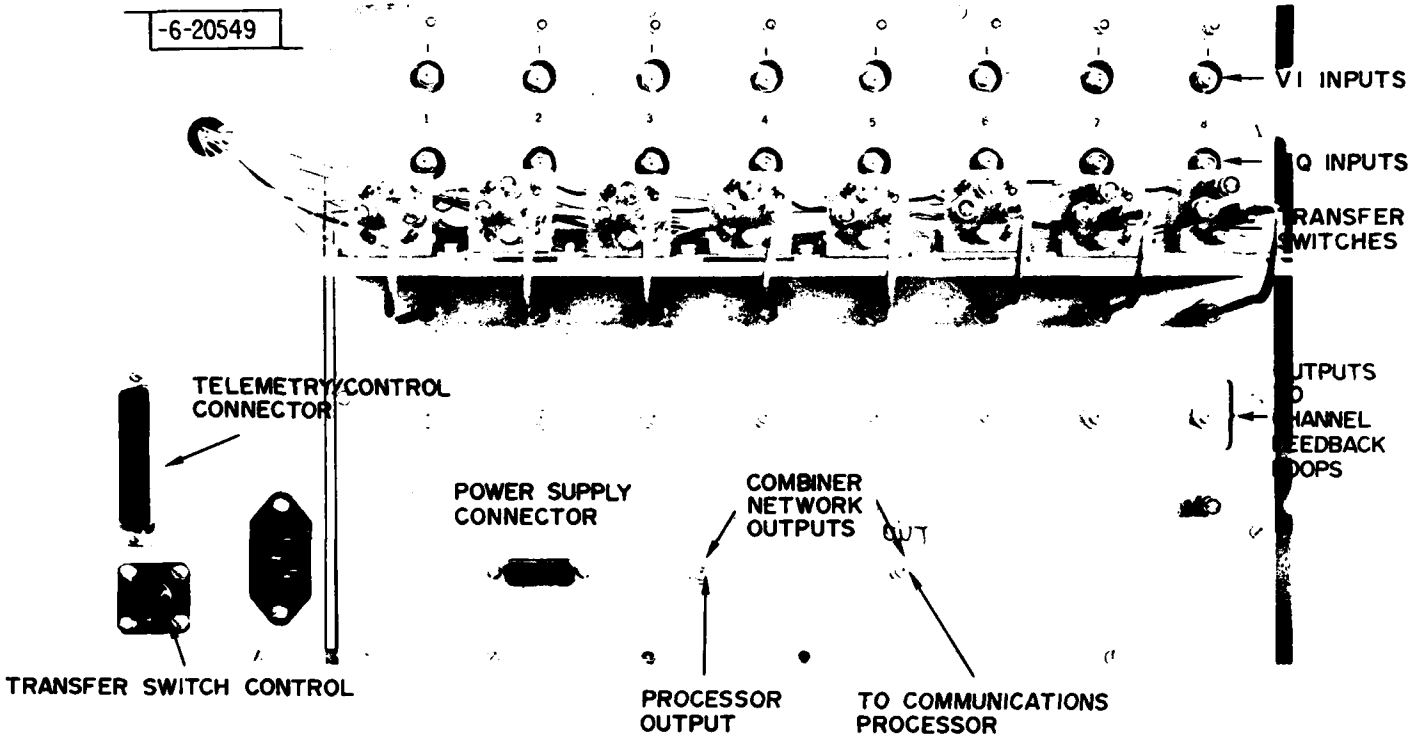


Fig. 3.3. Rear-view of Weight and combiner network assembly (A13) showing input/output connections.

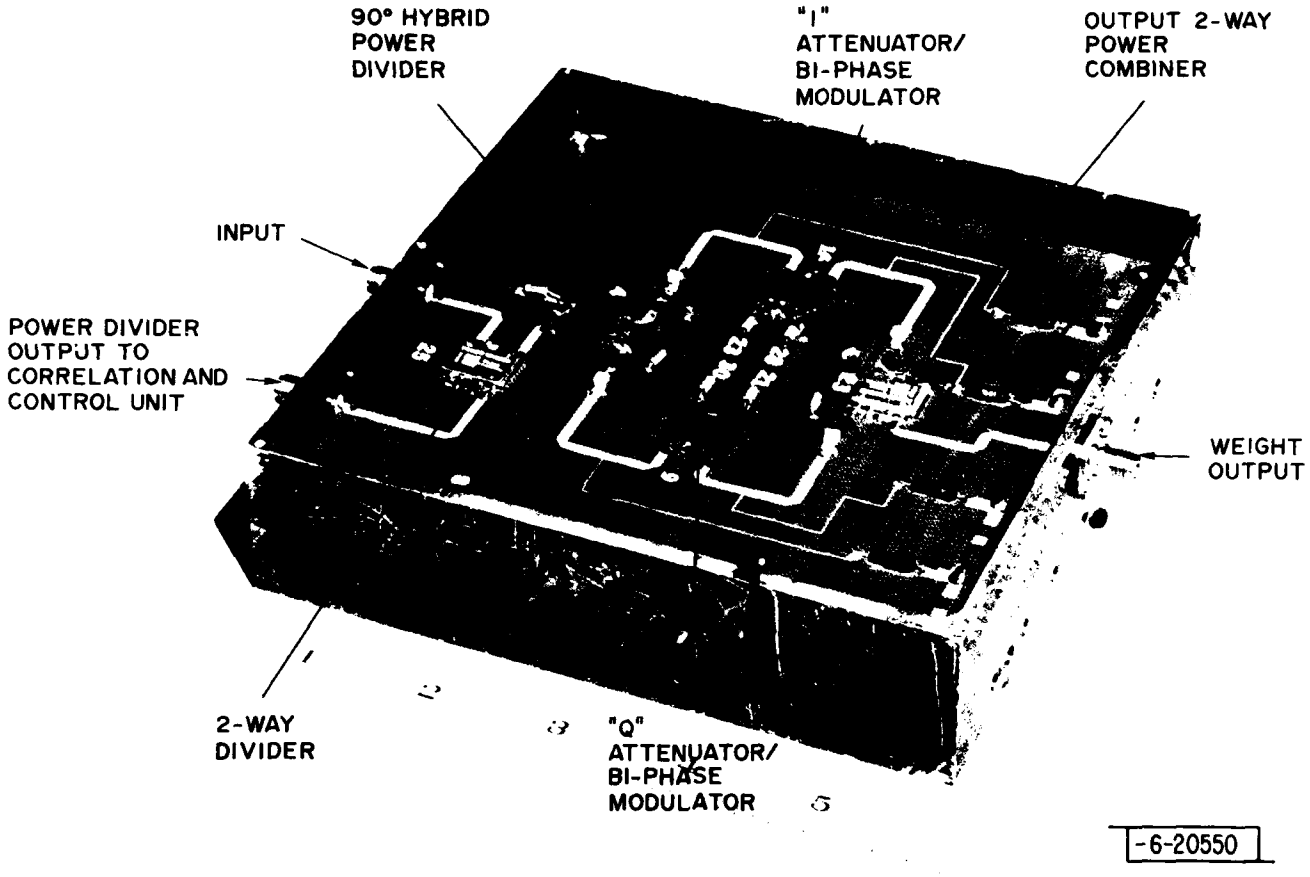


Fig. 3.4. Narrowband PIN diode weight circuit with top cover removed.

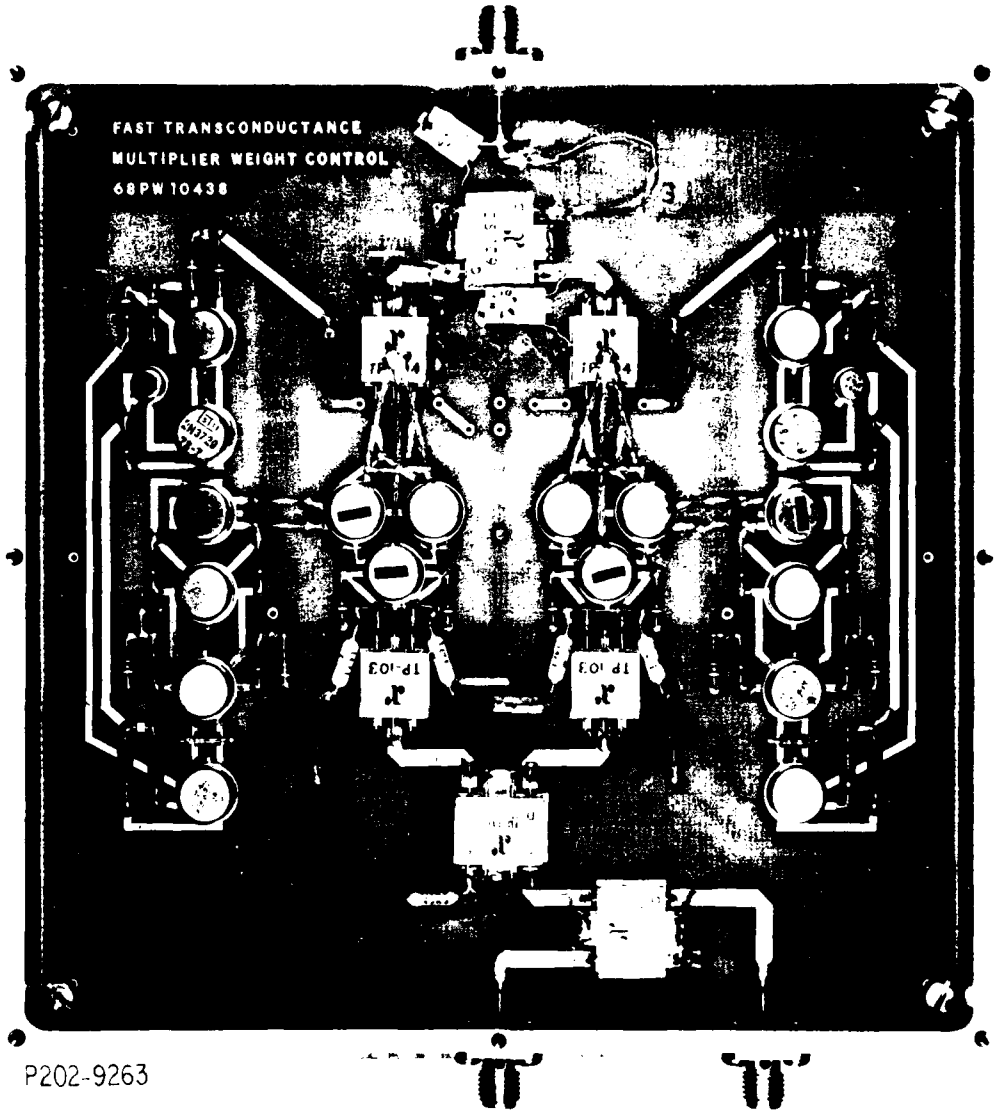
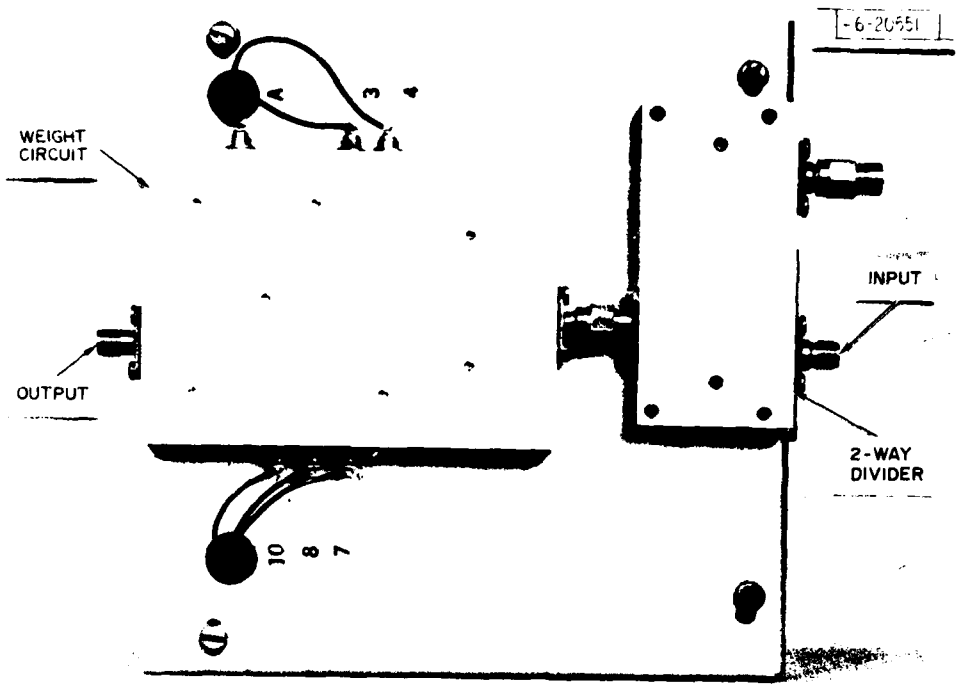


Fig. 3.5. Transconductance multiplier weight with top cover removed.



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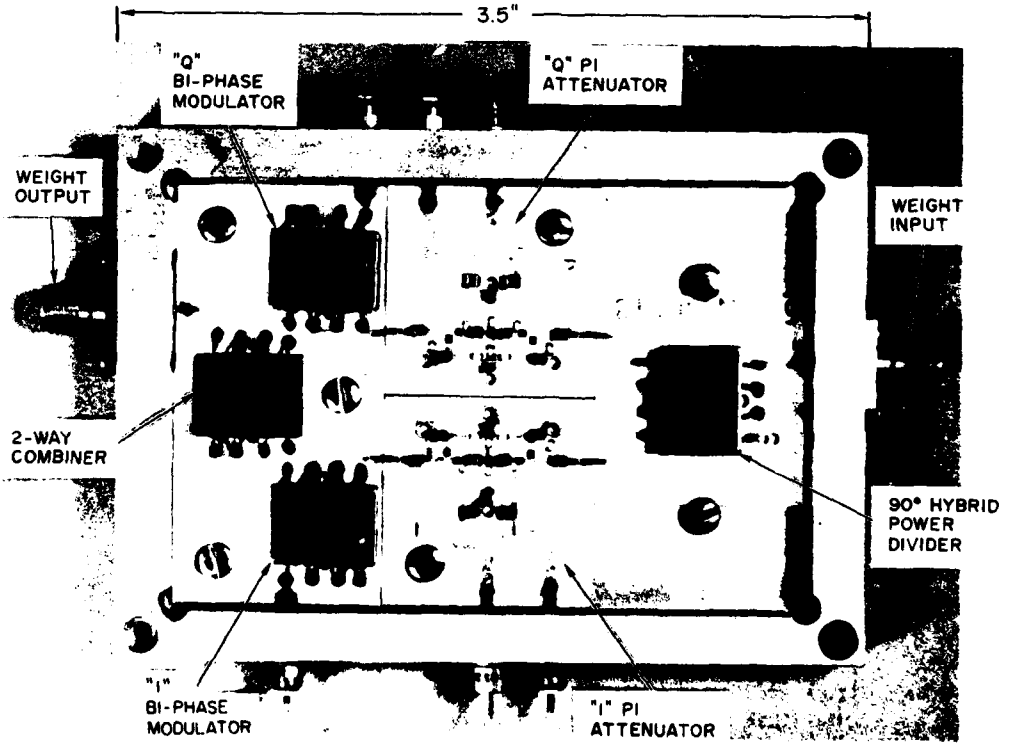

(b)

Fig. 3.6. Broadband PIN diode weight module.

different in that the two-way power divider, the weight circuit and the weight driver were each assembled separately and later interconnected and mounted to a flat plate having the same exterior dimensions as the previous weight modules.

3.2.2 Combiner Network

The combiner network, shown in Fig. 3.7, consists of an eight-way combiner fabricated from a corporate arrangement of two-way power dividers, with a hybrid power divider connected to the output of the combiner to separate the combined signal into two output signals. One of the two output signals is used by the Correlation and Control unit (A7) for the control of the feedback loops; the other output signal was included to allow for the capability of connecting communications processing equipment or test equipment to the output of the processor.

During the process of fabricating the combiner network, several steps were taken to minimize channels mismatch errors. First, each power divider was measured and only those having well matched characteristics were used in the final assembly. Secondly, as a means for equalizing differences in the phase slope (i.e., the phase vs frequency) between channels, small amounts of shunt reactance were added to selected channels of the combiner. In this way it was possible to change the phase and, to some extent, the amplitude response of each channel in very small amounts. By adjusting each channel transfer function in this manner, it was possible to achieve an RMS channel mismatch error of less than 0.01 dB and 0.1° over a 50-MHz bandwidth.

3.2.3 Telemetry Control and Monitor Network

The telemetry and control link* with the Weight and Summer Network (A13) is handled by a specially designed interface card resident in A13. The card consists of a series of analog multiplexers which are controlled by the Telemetry and Control unit (A1) to allow any one of 64 test points within A13 to be selected and returned to A1 for display. The 64 test points represent

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*Additional information on the TLM/CMD link is provided in Section 8.2 of this document.

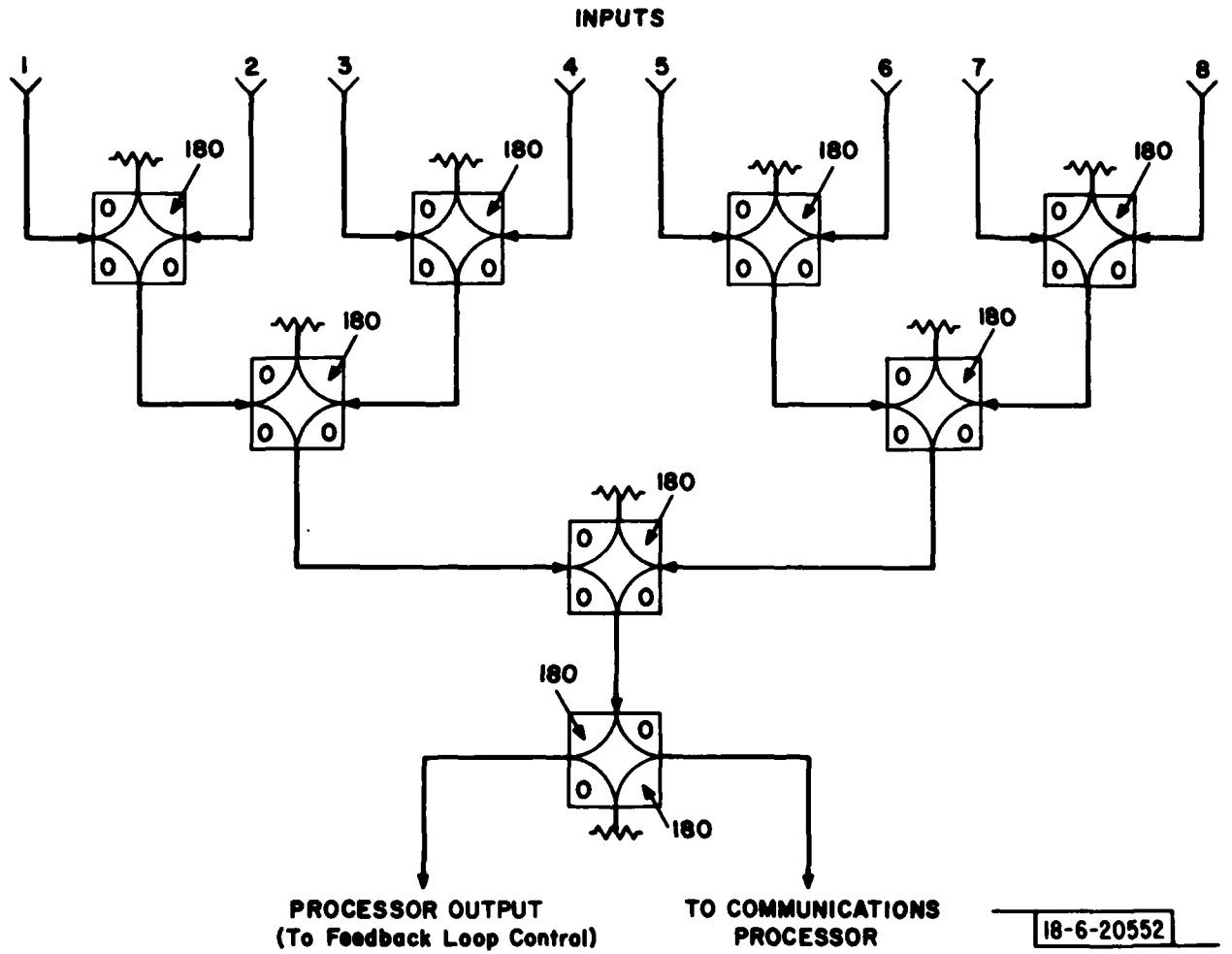

Fig. 3.7. Combiner network schematic diagram.

8 test points for each of the 8 weight modules, corresponding to 4 "I" and 4 "Q" test points per weight. These test points include variables such as the weight control voltages generated by the Correlation and Control unit (A7), PIN diode voltages and other reference points within the weight driver circuits.

The telemetry interface card also contains the drivers for actuating the channel transfer switches. The control of the channel transfer switches is provided by A1, with the dc power requirements of each switch and indicator lamp (+28V @ $\sim$ 200 mA per channel) supplied by a power supply located on a shelf behind A13.

The weight monitor circuit provides the capability of selectively monitoring and displaying on the front panel of A13 any one of the 64 telemetry test points. An additional feature provided by the monitor circuit is the capability of disconnecting the weight control voltages generated in A7 and substituting in its place dc control voltages from the reference circuit. This capability has been found quite useful, for example, as a troubleshooting aid in debugging and identifying hardware-related problems. It is also useful as a means for conditioning the weight (by setting, say, $V_I = 1$, $V_Q = 0$ volts) and measuring, with the aid of a network analyzer, the channel transfer functions for determining the relative channel mismatch errors.

The controls for the weight monitor are located on the right-hand front panel of A13. Using these controls one can select any one of the eight weight circuits and any one of the 64 test points for display on the front panel LED display. Separate controls are provided for changing and displaying the V_I and V_Q control voltages to each weight circuit.

3.3 Channel Matching Performance

As a final step in evaluating the WSN, a series of tests was conducted to determine how closely the individual channel transfer functions match each other in amplitude and phase vs frequency. In this section, we present two general techniques which have been found quite useful as a means for quantifying channel matching, and present along with those discussions, measurement data to illustrate the channel tracking performance of the WSN assembly.

3.3.1 Method 1 — Channel Mismatch Errors

In the first method, channel matching performance is described in terms of the channel mismatch errors occurring between the transfer function of each channel and a reference transfer function. Although the choice of the reference is arbitrary, for this discussion we choose it to be the transfer function of channel 1. Letting $H_i(\omega)$ and $\phi_i(\omega)$ represent the amplitude and phase, respectively, of the i^{th} channel vs frequency, we define the amplitude mismatch, $\delta_i(\omega)$, and the phase mismatch, $\alpha_i(\omega)$, as

$$\begin{aligned} \delta_i(\omega) &= \left|1 + \frac{H_i(\omega) - H_1(\omega)}{H_1(\omega)}\right| \\ \alpha_i(\omega) &= \phi_i(\omega) - \phi_1(\omega) \end{aligned} \tag{3.1}$$

Since fixed offsets between channels, either in amplitude or phase, do not contribute to channel mismatch, it is useful to rewrite Eq. (3.1) by setting both offsets to zero at $\omega = \omega_o$, viz,

$$\begin{aligned} \delta_i'(\omega) &= \delta_i(\omega) - \delta_i(\omega = \omega_o) \\ \alpha_i'(\omega) &= \alpha_i(\omega) - \alpha_i(\omega = \omega_o) \end{aligned} \tag{3.2}$$

Next we compute from Eq. (3.2) the rms amplitude and phase mismatch errors,

$$\begin{aligned} a(\omega) &= \sqrt{\frac{1}{(N-1)} \sum_{i=2}^{N} [\delta_i'(\omega) - \delta_o'(\omega)]^2} \\ \Delta(\omega) &= \sqrt{\frac{1}{(N-1)} \sum_{i=2}^{N} [\alpha_i'(\omega) - \alpha_o'(\omega)]^2} \end{aligned} \tag{3.3}$$

where

$$\delta_o'(\omega) = \frac{1}{N-1} \sum_{i=2}^{N} \delta_i'(\omega)$$

$$\alpha'(\omega) = \frac{1}{N-1} \sum_{i=1}^{N} \alpha_i'(\omega) \qquad (3.4)$$

are the average amplitude and phase mismatch errors.

To demonstrate this technique, Fig. 3.8 shows the measured channel mismatch errors (i.e., Eq. (3.2)) for the combiner network, plotted as a function of frequency over a 50-MHz bandwidth. In this case, the amplitude and phase mismatch errors are all quite small, uncorrelated, and essentially independent of frequency, indicating that all channels are very closely matched over the 50-MHz bandwidth. The excellent tracking performance of the combiner network is due largely to the fact that the power dividers used in constructing the combiner have a large bandwidth ($\sim$ 500 MHz), and consequently have frequency characteristics which change little over the 50-MHz measurement bandwidth. This makes the task of matching channels much easier and permits lower levels of mismatch errors to be achieved with relatively simple techniques. As shown in Table 3.1, the rms channel mismatch errors for the combiner network, computed from Eq. (3.3) are less than 0.1 dB and 0.05 degree over 50 MHz.

TABLE 3.1

RMS CHANNEL MISMATCH ERRORS VS
BANDWIDTH FOR THE COMBINER NETWORK

Bandwidth (MHz)	RMS Channel Deviations (dB)	(Degrees)
10	0.005	0.04
20	0.005	0.04
30	0.005	0.04
40	0.005	0.04
50	0.005	0.04

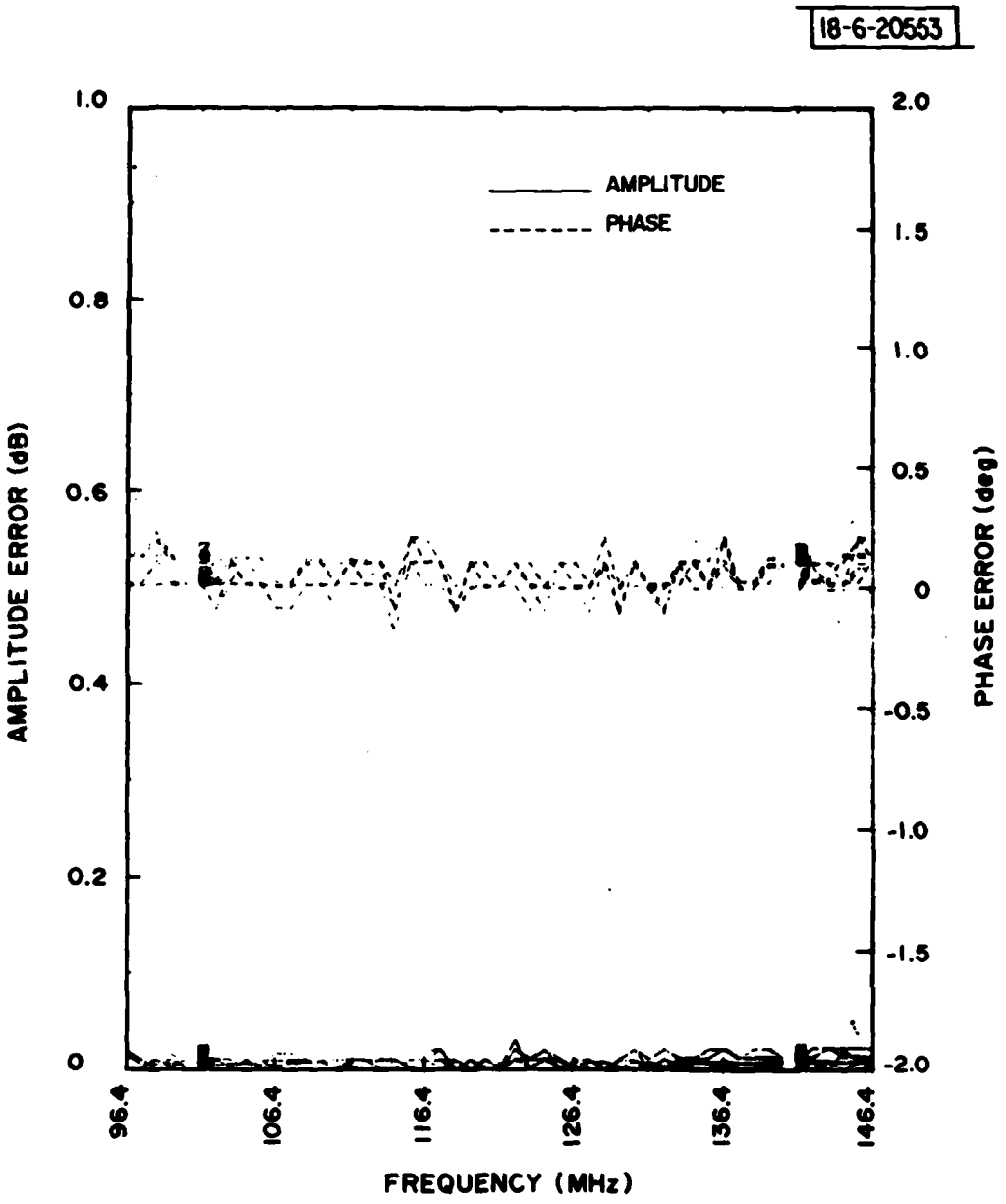

Fig. 3.8. Amplitude and phase channel mismatch errors for the combiner network.

In contrast to the combiner network in which the channels were relatively easy to match, the Weight and Summer Network presents a more difficult task since it includes not only the combiner network, but the weight modules, transfer switches and interconnecting cables, all of which must be matched from channel to channel. In addition, the weight circuits must operate over a large dynamic range and therefore are required to be matched not only for a particular weight setting, but for all possible weight settings. In other words, the characteristic tracking performance of the weight circuits should not change or vary to any great extent with either attenuation and/or phase. This, however, was not the case, and it was found that, in general, the tracking performance of all three sets of weight circuits exhibited some degree of variation with weight setting. The narrowband weight circuits exhibited the poorest overall performance in terms of their tracking performance, apparently as a result of the relatively small dynamic range of the weight attenuator circuits ($\sim$ 35 dB) which gives rise to correlated output signals down 35 dB or less from the input level. The transconductance weights and broadband PIN diode weight circuits, on the other hand, demonstrated much better tracking performance at a level approximately 12 dB better than the narrowband weight circuits (see next section). As a means for demonstrating the tracking performance of the WSN assembly, Figs 3.9, 3.10 and 3.11 illustrate the tracking data [i.e., Eq. (3.2)] for the broadband PIN diode weight circuits at three values of control voltages. In each case, the channel transfer functions were measured from the input to the transfer switch through each channel to the output of the combiner network. The three cases clearly demonstrate that certain channels in general tend to be more closely matched to the reference channel (i.e., channel 1) than others, but that the specific channel(s) which match best varies with weight setting. Also apparent from Figs. 3.9, 3.10 and 3.11 is the fact that the tracking errors are much more correlated and frequency dependent, unlike the combiner network where the tracking errors were found to be uncorrelated and more frequency independent. As shown in Table 3.2, the rms tracking errors for the WSN assembly tend to average less than 0.01 dB and 0.1° over the 10-MHz IF bandwidth.

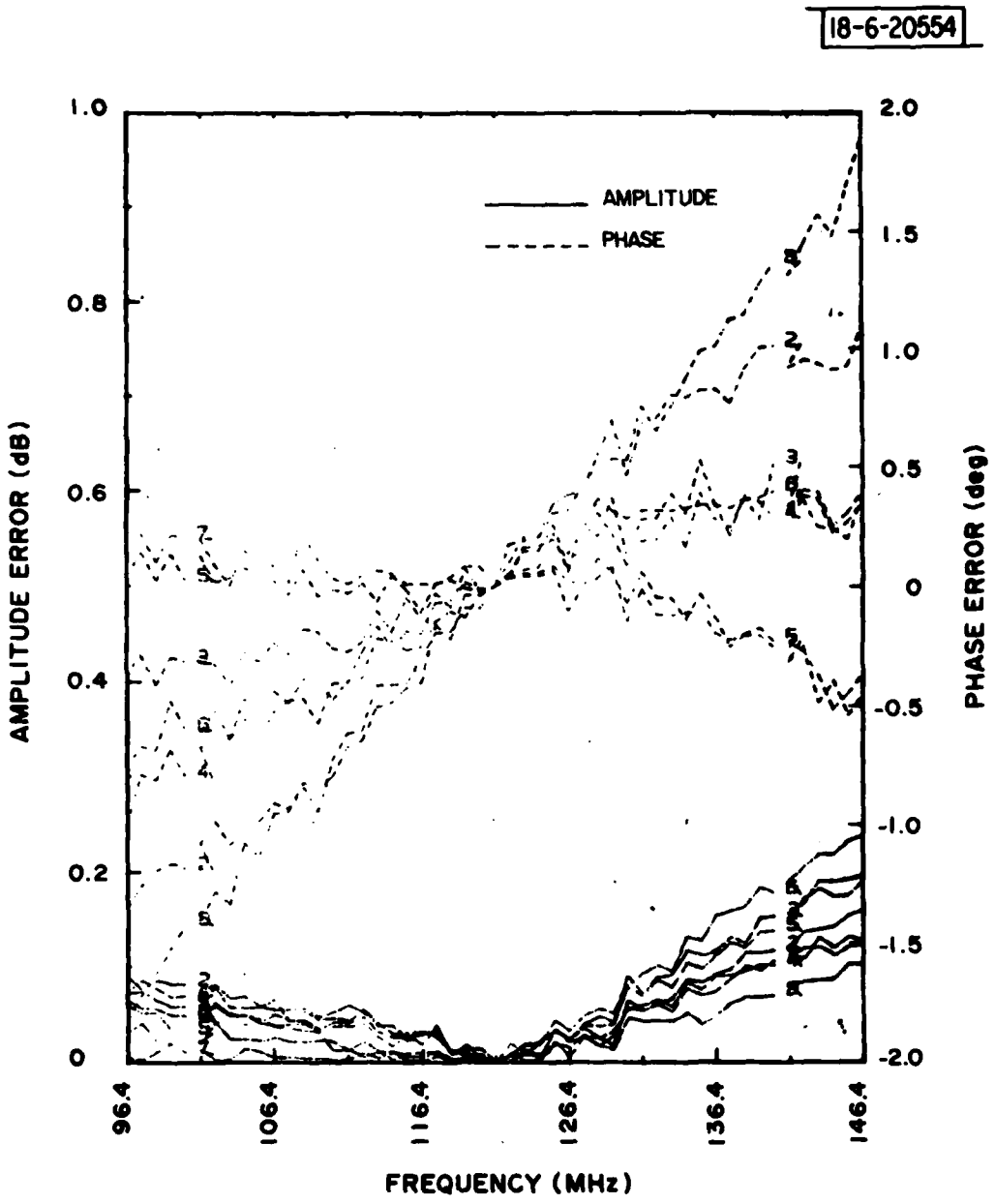

Fig. 3.9. Amplitude and phase channel mismatch errors for the WSN assembly with V_I = -1 and V_Q = -1 volt.

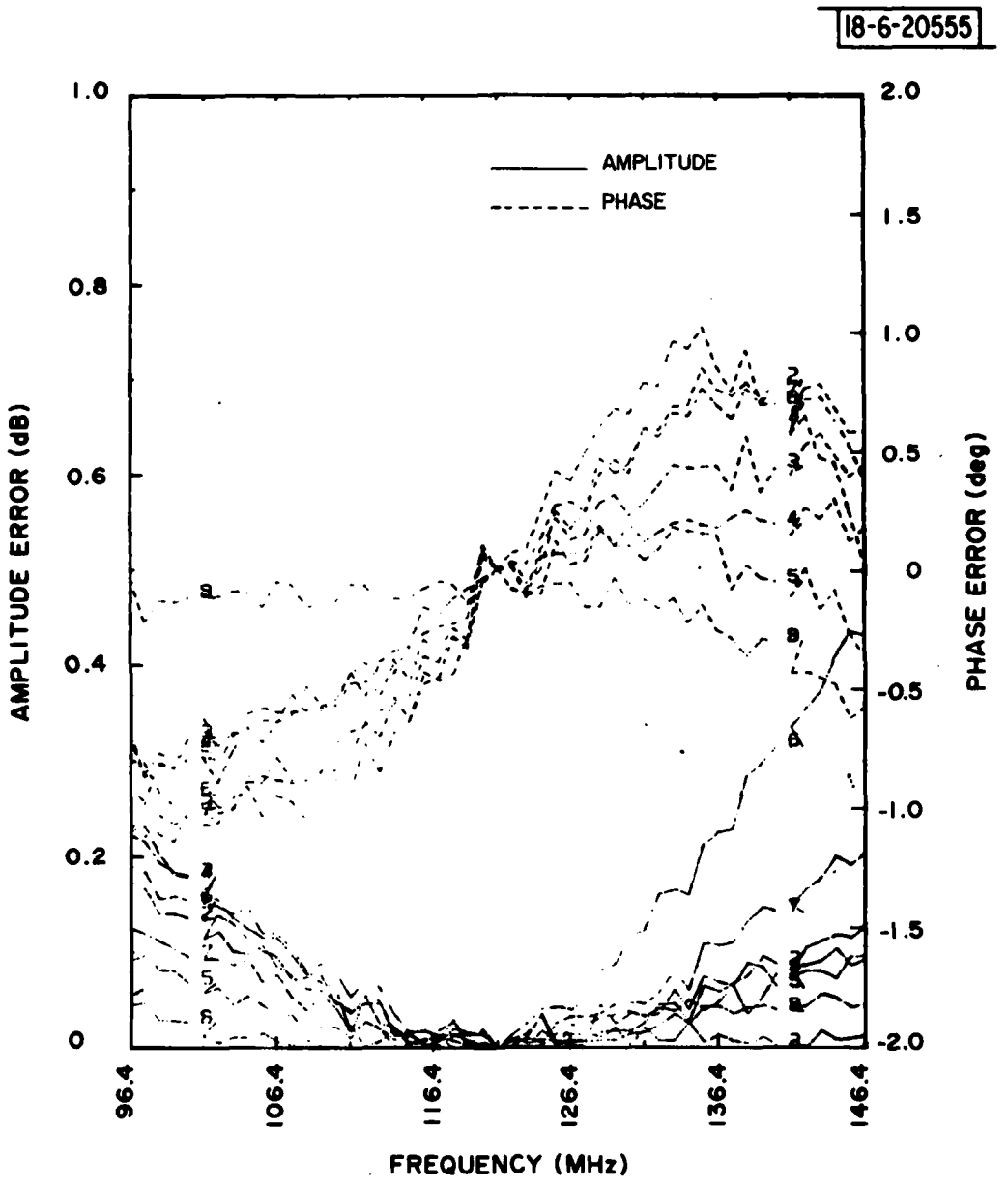

Fig. 3.10. Amplitude and phase channel mismatch errors for the WSN assembly with V_I = 0 and V_Q = -1 volt.

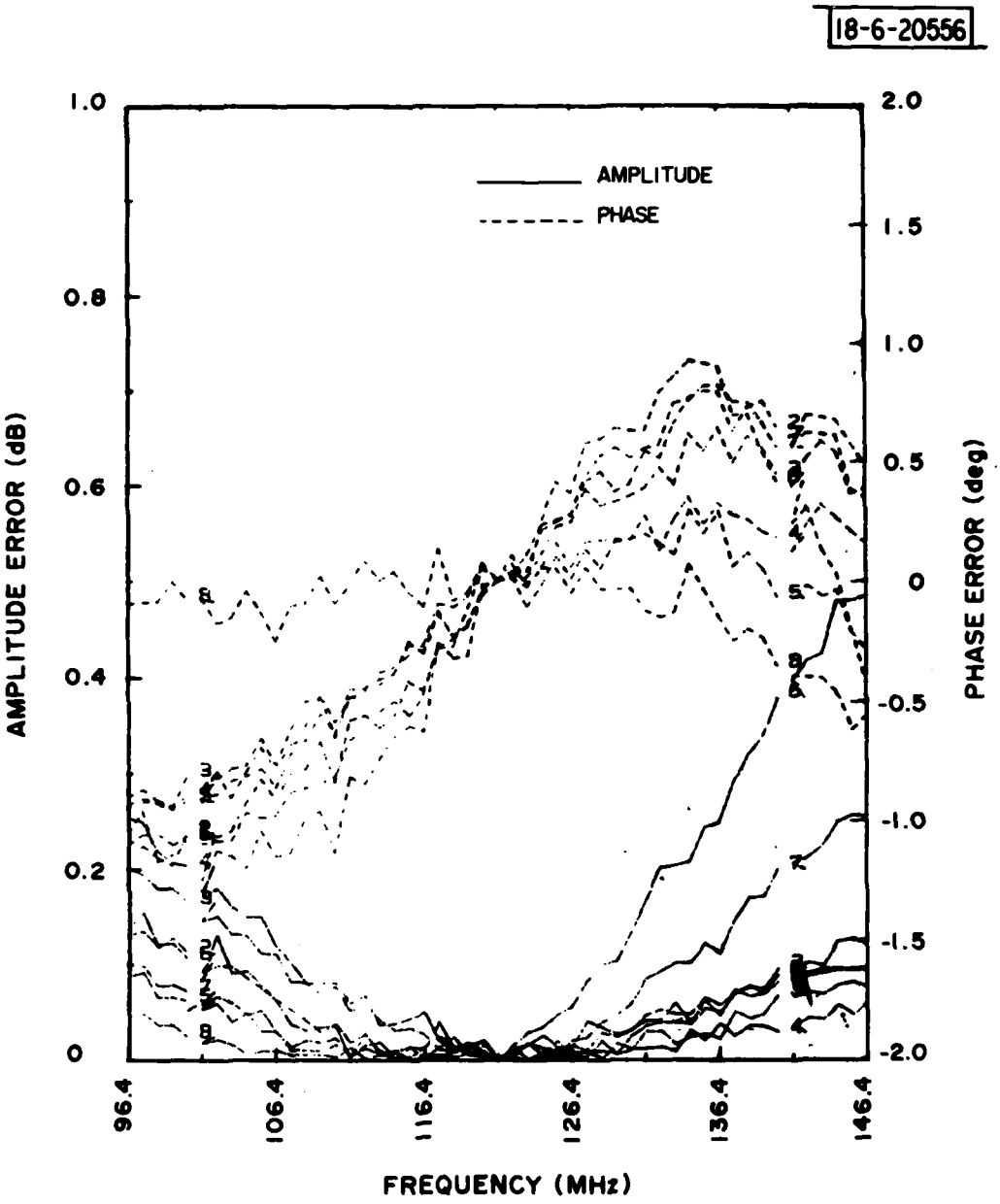

Fig. 3.11. Amplitude and phase channel mismatch errors for the WSN assembly with V_I = 0 and V_Q = 1 volt.

TABLE 3.2

RMS MISMATCH ERRORS VS BANDWIDTH AND WEIGHT CONTROL VOLTAGE SETTINGS FOR THE WSN ASSEMBLY*

Bandwidth (MHz)	RMS CHANNEL ERROR					
	$V_I = -1$, dB	$V_Q = -1$ Degrees	$V_I = 1$, dB	$V_Q = 1$ Degrees	$V_I = 0$, dB	$V_Q = 1$ Degrees
10	0.007	0.08	0.008	0.07	0.011	0.09
20	0.011	0.15	0.013	0.13	0.021	0.15
30	0.015	0.21	0.017	0.14	0.034	0.20
40	0.018	0.27	0.023	0.24	0.048	0.22
50	0.022	0.33	0.027	0.30	0.062	0.23

*Measured using broadband PIN diodes.

3.3.2 Method 2 — Eigenvalue Analysis

A second, somewhat more esoteric method for determining channel matching, is based on first computing an N × N average covariance matrix, $\underline{\underline{R}}$, from the measured N channel transfer functions according to

$$\underline{\underline{R}} = \frac{1}{FBW} \int_{1-\frac{FBW}{2}}^{1+\frac{FBW}{2}} H_k(\omega) H_q(\omega) dW \qquad k, q = 1, 2, \ldots, N \tag{3.5}$$

where H_k is the (complex) transfer function of the k^{th} channel, ω_0 denotes the center frequency, $W = \omega/\omega_0$ and FBW is the fractional bandwidth about ω_0. From $\underline{\underline{R}}$ one then computes, from the equation,

$$\underline{\underline{R}} \cdot \underline{e}_k = S_k \underline{e}_k \qquad k = 1, 2, \ldots, N \tag{3.6}$$

a set of eigenvalues, S_k, and their corresponding eigenvectors, $\underline{e}_k$. In Ref. 12, it is shown that the channel tracking characteristics can be determined directly from the eigenvalues of $\underline{\underline{R}}$ by considering the eigenvalues as parametric functions of the bandwidth over which $\underline{\underline{R}}$ is formed. Specifically, when FBW = 0 there is only one non-zero eigenvalue, $S_1 = S_{MAX}$, which can be interpreted as representing the total power out of the N channels when the eigenvector corresponding to S_{MAX} is applied as weights in the channels. The remaining eigenvalues all yield zero output power (theoretically) when applied as weights. As the bandwidth increases the lower eigenvalues begin to increase (i.e., $S_2, S_3, \ldots, S_N > 0$) and, in fact, arise as a direct result of mismatches between channel transfer functions. Therefore, by observing the behavior of the eigenvalue spectrum, one can infer the tracking performance and bandwidth behavior of the channels.

The principal case of interest here is one in which all weight circuits have the same control voltages; in this case the cancellation dependence can be determined from the first two eigenvalues (Ref. 12), according to

$$C = K\left(\frac{S_2}{S_{MAX}}\right) \tag{3.7}$$

where K is a constant depending on the steering vector and angle of arrival. Generally, $K \leq N$ where N is the number of elements. Figure 3.12 shows a comparison of the eigenvalue ratio (S_2/S_{MAX}) obtained with the WSN assembly for each set of weights. The usefulness of Fig. 3.12 is that it not only indicates the approximate level of cancellation which can be achieved with each set of weights, but it also provides in many cases some insight into the nature of the mismatch errors and allows a tradeoff to be made between differing types of weights. In Fig. 3.12, for example, it can be observed that the eigenvalue ratio decreases approximately 6 dB for each octave increase in frequency which suggests that the primary mechanism contributing to channel mismatch has a bandwidth square dependence. One particularly important class of errors which exhibit this type of behavior (i.e., $C \sim BW^2$) is path length errors (time delays) in the signal paths which lead to highly correlated mismatches between channels. These types of errors are present in almost

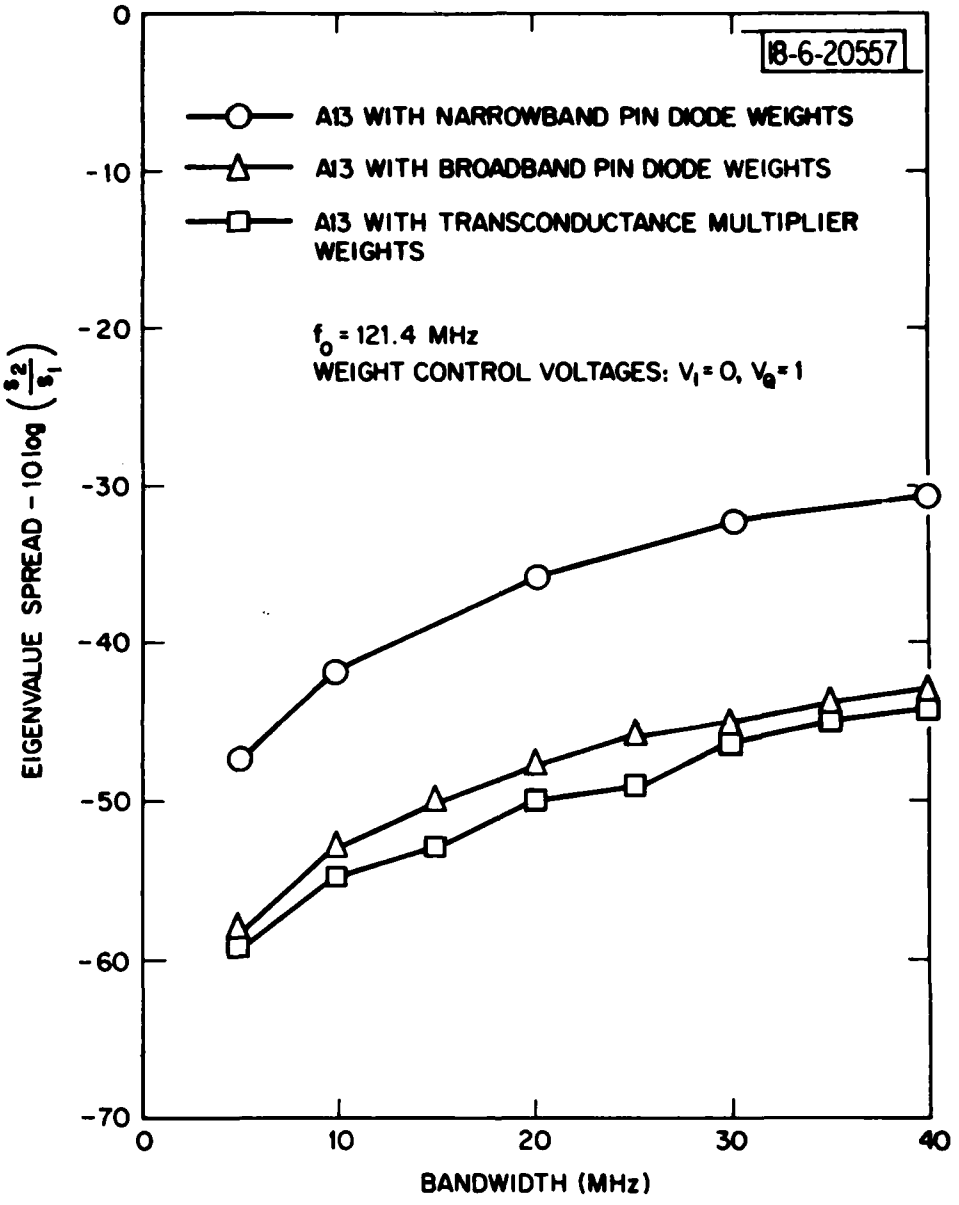

Fig. 3.12. Eigenvalue ratio (S_2/S_{MAX}) vs. bandwidth for the weight and summer network (A13) with the three sets of weight circuits.

any type of system and can occur for a variety of reasons ranging from differences in the physical path lengths of the channels to impedance mismatches which give rise to multiple reflections and hence multiple time delays. For the narrowband PIN diode weights, it was determined that the principal factor limiting tracking performance was in fact a time delay difference between the desired weighted signal and an undesired, non-weighted "leakage" signal which occurs at the weight output as a result of the finite isolation ($\sim$ 35 dB) of the weight attenuator circuits. Although the other two sets of weight circuits exhibit the same type of frequency behavior as the narrowband PIN diode weights, their performance is significantly better ($\sim$ 12 dB), making the task of identifying mismatch errors more difficult. For these two sets of weight circuits, the channel mismatch errors are most likely due to a combination of small time delay errors resulting from "leakage" signals and impedance mismatches.

The weight circuits are described in greater detail in Technical Note 1979-11 (Table 1.1).

IV. CORRELATION AND WEIGHT CONTROL

4.1 Introduction

A Correlator in the general sense of the term is simply a device which is capable of measuring the amount of coherence between two signals. In this section, however, "correlators" shall not only include circuits which perform the above-mentioned task, but also the appropriate filtering, buffering, summation, and other auxiliary functions which eventually provide signals to a set of controllable weights.

In a nulling system where there are N identical channels, all channels pass through a set of complex weights and are eventually summed to produce a single output. The first job of the correlator is to provide N complex signals which, for a given system bandwidth, provide real-time estimates of the degree of correlation between the sum signal and the N channel response which are observed ahead of the weight circuits. In this system, correlation is done at an IF frequency of 121.393 MHz with a 10 MHz bandwidth. For noisy inputs, the variance of the correlator output is proportional to the system bandwidth. Consequently, since it is desired to measure the DC output of the correlator, the system bandwidth following this point should be no greater than 0.5 MHz to 1 MHz.

An additional function of a correlator is to provide real-time control signals to channel weights to provide the desired amount of decorrelation in the closed loop condition. In this system all correlators were implemented with in-phase (I) and quadrature (Q) steering voltages which are capable of modifying the static and dynamic weight settings. The I and Q steering voltages are simply added directly to the control signals just prior to application to the weights. In this system a first order loop was desired; hence, a single pole filter was used. A first order loop has certain drawbacks, but its performance is predictable and it is quite tolerant to system phase errors and amplitude unbalances. A second order system was contemplated, but eventually discarded due to potential stability problems coupled with inadequate available testing time.

One final point should be made. There is a need for time delay and phase matching of all lines to the correlator with the point of individual channel sampling used as the reference. That is, each of the N channels has a 2 way power splitter prior to the weight circuits. One output of the splitter eventually makes its way to one of the N "reference" inputs. The other input passes through the weights, into a summer, and eventually is split 8 ways to be processed by the linear "sum" side of each correlator. These two paths are the ones which must be time delay matched and phase aligned. Since in general only time delays can be adjusted by adding cable length, phase matching must be accomplished by including similar components in each path.

4.2 Design Considerations

In any practical system, the ultimate design goal is to eventually recover information from the N summed outputs. The design of the "straight through" system will usually dictate those gains distributions, 3rd order intercepts, and noise figure required. The designer is left, then, with a partially specified system which will have a gain and noise figure specification to the N individual sample points preceding the weight circuits as well as a similar specification to the summed output, assuming no channel to channel correlation. From these points, the remaining system gain to the correlators must be determined as well as the internal correlator gain and dynamic bandwidth.

There are several possible ways to determine the amplification required to complete the specification. The approach taken in this design was to work from the threshold point. The threshold point is defined as that set of inputs which when inserted into the front end of the N channels produces an effective 3 dB null on the interference. Since the range of interference inputs was specified as 20 dB to 60 dB above system noise, it was convenient to work with the 20 dB above noise threshold. One fact which makes gain computation difficult at threshold is that these are an endless number of possible N channel inputs which could be 20 dB above system noise. In general, all channels will be coupled and the problem of analytically uncoupling

them for design purposes becomes extremely difficult. An obvious choice, therefore, is to work at system noise levels for the threshold and then decrease the overall gain by 20 dB. This has the advantage that with system noise only, all N channels are decoupled; therefore, the system is diagonalized and computations can proceed on an individual channel basis.

The system design, then, follows the general procedure outlined below. First, assume the weights are set to a magnitude of one ($W_I^2 + W_Q^2 = 1$). Next, assume the sum channel output is a sine-wave whose magnitude is equal to the system noise at that point and that the system noise is reduced to zero. This sine-wave should be at band center (121.393 MHz in this case) and may have arbitrary phase. Further, a similar sine-wave should replace the output from the individual channel sample (2 way power splitter output). As a final step, the output is computed all the way to the I and Q weight control voltages and the IF and DC gains are set so as to give voltages which would produce a correlator output corresponding to a weight setting of magnitude one. In general, the IF gains are determined by the linear operating region of the multiplier (mixer in this case) used for the correlation portion. The remaining gain will be in the DC circuitry. All that remains in the gain setting is to reduce the overall amplification by 20 dB to push the threshold 20 dB above system noise.

The above discussion describes a method to determine the desired gains for the closed loop control system. Obviously other factors need to be considered. A good IF design will insure that noise figures are preserved and the channel bandwidths are not reduced or affected by IF components. The DC circuits also have bandwidth considerations. The residual time constant of the system is set by the low-pass circuitry in the DC portion of the correlator. This is the rate at which the system would relax from a given set of weights back to the quiescent state when the input is turned off. In this system that time constant was chosen to be 13.3 msec, the same as the hop interval. The input dynamic range requirements, however, modify the response time considerably. An 80 dB dynamic range of input power level would mean a

decrease in response time of 10^4 or 1.33 μsec for the largest set of inputs.* This corresponds to a bandwidth of 120 kHz over which the control circuits must operate and not introduce extraneous phase shifts or amplitude errors. This is obviously of concern when deciding what components to select for the DC part.

4.3 IF Equipment - Implementation and Rationale

In any set of equipment which claims to be a correlator in real time an item worthy of close scrutiny is the multiplier. In the ideal case, if A and B* are two complex input signals, the multiplier would form the product AB* so that complex outputs would be

$$\text{Re} = E[|A||B| \cos(\angle A - \angle B)] \quad \text{and}$$

$$\text{Im} = E[|A||B| \sin(\angle A - \angle B)] \quad .$$

In practice, components which could form products such as those expressed above are limited, especially since they must work at IF frequencies of 121 MHz. Transconductance multipliers might be able to do the job, but the technology is difficult to achieve. Another consideration is that if A and B have a 40 dB dynamic range, then clearly the product could have an 80 dB dynamic range. So, for a linear component, such as a transconductance multiplier, the component dynamic range would be twice the system dynamic range (on a dB scale). Mixers are another "multiplying" component. They are readily available at almost any frequency but they are nonlinear. The LO input must always be amplified up to a constant level either through limiters or AGC circuitry. These components, therefore, have dynamic range requirements similar to those of the system. In this nonlinear case, the multiplier output products would be

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*These results are dictated by the hard-limiter present in the feedback path from element output to correlator input.

$$\text{Re} = E\left\{\frac{|A||B|}{|A|}\cos(\angle A - \angle B)\right\} \quad \text{, and}$$

$$\text{Im} = E\left\{\frac{|A||B|}{|A|}\cos(\angle A - \angle B)\right\} \quad .$$

In the case of 8 channels derived from a phased array antenna, all the associated inputs would have the same general magnitude. Consequently, for mixers as multipliers, the system response in the presence of a single interference source would be similar except for a magnitude scale factor.

In the system implemented, mixers were chosen for the multiplier and as far as dynamic range was concerned, they were the main limiting factor. Dynamic range here means the range of inputs which could be applied to the system and still preserve linearity. Figure 4.1 shows a dynamic range in excess of 40 dB with the high end limit due to the mixer itself. Referring to the overall system detailed block diagram (Fig. 1.3) these mixers are shown interconnected with 0/180° and 90° hybrids to implement real and imaginary (in-phase and quadrature) components. The dynamic range of greater than 40 dB over threshold also takes into account measurements of the low frequency response of the circuits which will be discussed later. This threshold can be adjusted upward, however. Referring to Fig. 1.3, in series with the summed output there is a 15 dB attenuator. This attenuator can be incremented in 5 dB steps (see Sec. VII), thereby reducing the loop gain by a similar amount. This does imply, however, that preceding channel circuits are capable of handling at least 55 dB dynamic range instead of 40 dB.

The improved component dynamic range achieved by the use of the limiters is not without its problems. Isolation between the LO side of the mixer and the RF port must be high. The design point is such that the LO side is always maintained at approximately +8 dBmW. Since for linearity the mixer RF side should always be below -10 dBmW, the 40 dB dynamic range would place this value at no more than -50 dBmW. In practice the threshold to the mixer

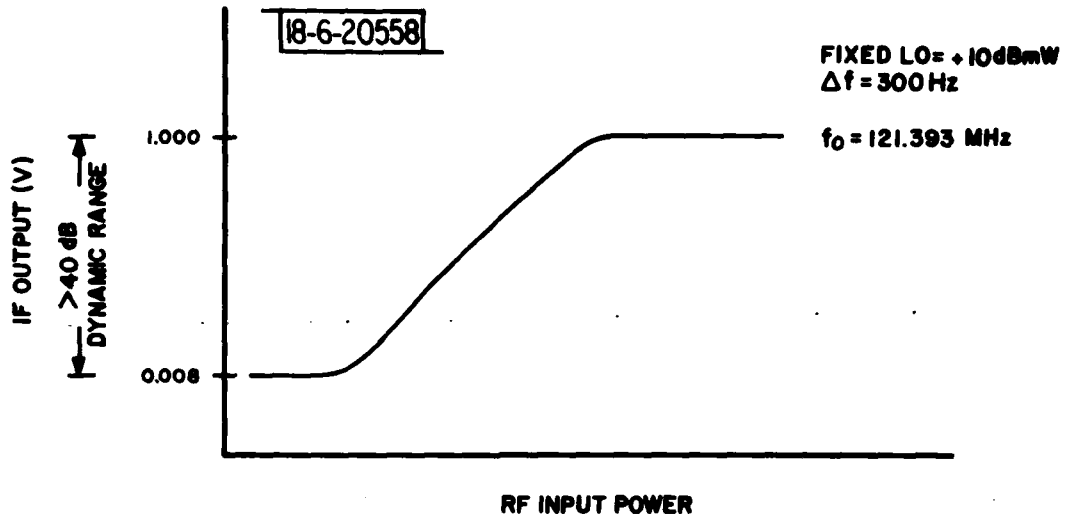


Fig. 4.1. Mixer linearity.

was set up at -53 dBmW. As the IF output is basically the result of mixing to baseband, LO self-induced DC outputs must be minimized. Suppose the LO to RF isolation were as small as 30 dB. Then a +8 dBmW LO signal would appear as an outgoing wave of -22 dBmW on the RF port. This signal would then reflect off the hybrid (with a typical return loss of 20 dB) and show up at the RF port as an incoming wave with magnitude -42 dBmW. This level is already 11 dB higher than the minimum expected signal and will cause a significant DC offset. Further, there is no guarantee that across the 10 MHz band the phase of this unwanted signal will not change, causing the self-induced DC voltage to vary. As a design point, then, it was assumed that the maximum LO power would be +10 dBmW with the desired level of self-induced power coming back into the RF port as 10 dB below the threshold of -53 dBmW. Using a typical return loss of 20 dB for the 0°/180° hybrid, the mixer isolation must be 53 dB or greater. In practice, hybrids were selected so that the return loss at each port exceeded 25 dB, and ultimately a manufacturer was found which could produce mixers with isolation greater than 50 dB.

The matching of the mixer ports was examined across the 20 MHz band centered around 120 MHz. This particular measurement did not involve entirely passive terminations, however. It was reasoned that a greater base-band dynamic range might be achieved by extracting the short circuit current from the mixers rather than terminating them with 50 Ω and amplifying the resultant voltage. So in effect, a non-uniform termination was selected such that the LO and RF ports of the mixer were terminated by 50 Ω; the IF port, via the diplexer, terminated the frequencies above approximately 10 MHz with 50 Ω and those frequencies above which the DC active network could not maintain an active short circuit. After much computation and experimentation, the circuit of Fig. 4.2 was selected using a 50 Ω resistor to terminate the diplexer for those frequencies for which the high speed op-amps following the diplexer could not sink the required current.

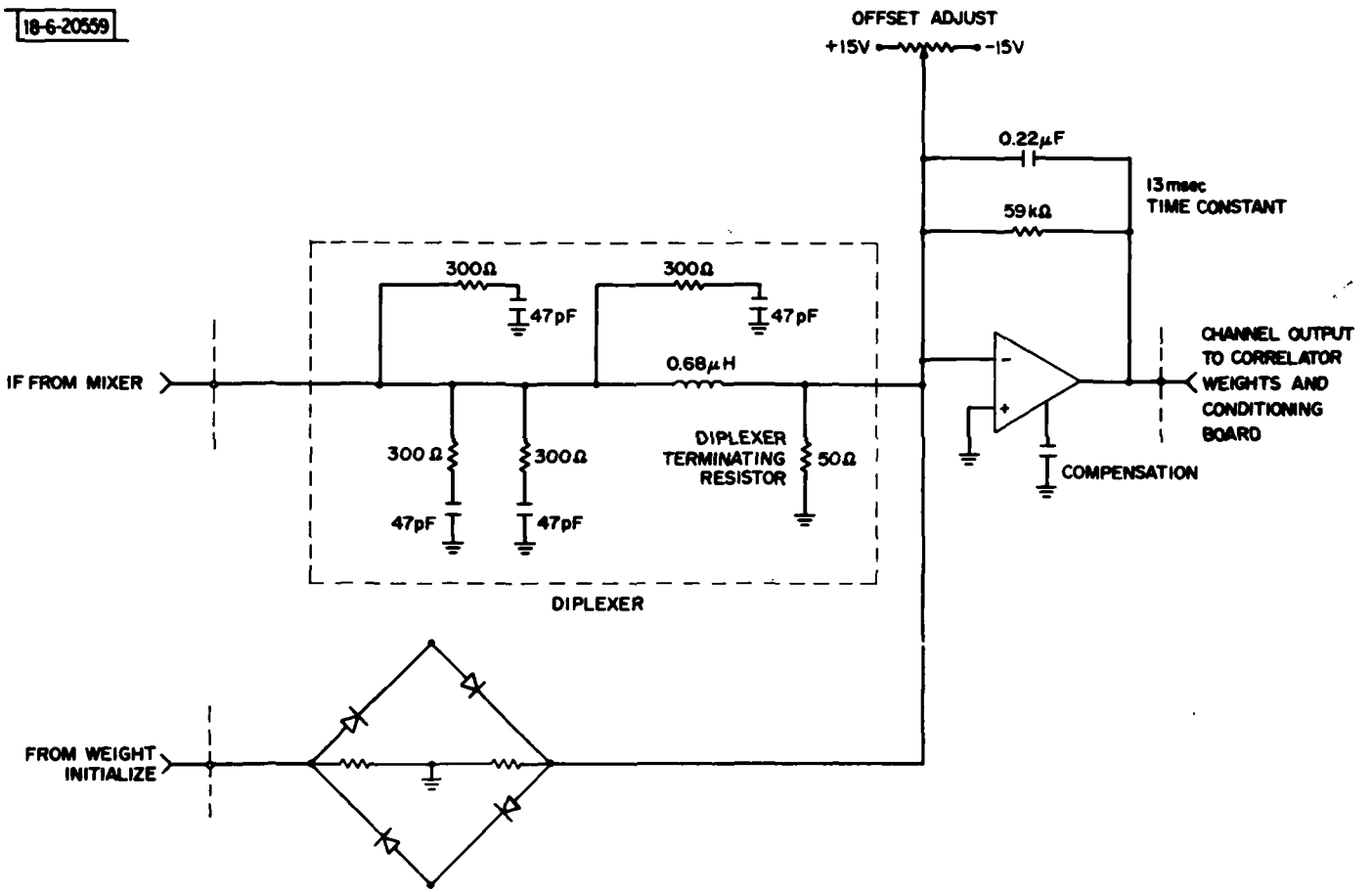


Fig. 4.2. Simplified schematic of the diplexer and amplifier board in the correlator module (I or Q channel).

The diplexer necessarily must terminate all frequencies of 100 MHz and above and pass all frequencies of 1 MHz and below. Hence, the crossover was designed at $\sqrt{100-1}$ MHz $\approx$ 10 MHz. In addition, it has to be examined for phase distortion at the upper end of the low frequency response of the control loop, in this case about 500 kHz. The required maximum phase shift at that point was specified at 5° and the circuit satisfied that objective.

Phase shifts as a function of frequency or power level were considered critical for all components of the system. One of the more critical components of concern was the limiter/amplifier. It is well known that as circuits saturate, the time delay tends to increase. In the normal operation of the limiter/amplifiers, they are required to produce a constant output for the mixers while the input varies in excess of 40 dB (see Fig. 1.3 for the configuration). As this delay variation is not matched by similar variations as a function of level on the sum side, differential phase shifts will exist with the mixers which cannot be eliminated. Fixed phase offsets in themselves are not a large problem for a first order loop as exists here; however, they should be minimized as much as possible. The limiter/amplifier was specified for an overall delay variation of 5° over a 50 dB dynamic input range with channel matching of this delay much better than 1° over the frequency band and power levels of interest. In practice, the overall delay variation specification was not met, but units were able to be selected which tracked each other very well.

From examining Fig. 1.3, it should be noted that after the hybrid which splits the channel signal off to the correlation and control circuitry, there are a number of similar components in the paths which eventually end up at each side of the quadrature mixers. One of these items is the hybrid. 0/180° hybrids are not of much concern as they exhibit a fairly flat time delay and can be equalized with appropriate cable length adjustments. The 0/-90° hybrids, however, could be somewhat different. If the quadrature hybrid is of the stripline variety, then the two outputs appear as two time

delays separated by 90° with approximately parabolic characteristics with regard to differential phase, loss above theoretical, and VSWR across the 20% frequency band. For a number of considerations, lumped 90° hybrids were used in the weight circuits. Again, these look like time delays separated by 90°. However, the differential phase is not nessarily parabolic; it could and frequently does have ripples in it over the band. Since ripples cannot be equalized by pure time delays, a pair of similar 90° hybrids was put into the other signal path (the channel sample) to help match the nonuniform phase characteristics. Again, refer to Fig. 1.3 and note that the item called variable gain actually contained a lumped element 90° hybrid in the first set of detailed tests. In the subsequent test, this was replaced with specially designed transconductance multipliers.

An even more critical item which has significant phase shift over the band of interest is the zonal filter. The zonal filter is required in the sum signal path to prevent a significant increase in noise figure. Coming out of the 8-way summer and after the split-off for the data channel, the net gain is only 7.6 dB, and the noise figure is 7.5 dB with the weights full on. The zonal filters must be designed carefully so that they are wide enough not to affect the system bandwidth, but narrow enough to prevent any appreciable out of band energy from reaching the 500 MHz wide amplifier which follows this circuitry. The minimum bandwidth desired was 25 MHz centered about 121 MHz. The actual bandwidth achieved -- taking into account the attenuation desired, the impedance matching required, the flatness across the band, as well as simplicity and realizability -- turned out to be closer to 45 MHz. Again, to match the non-uniform phase shift caused by the filter inserted in the sum channel, filters were added to all the channel sample paths. Since all of these needed to be matched over the channel bandwidth of 10 MHz, a nominal filter was selected in the sum channel. Then, on a network analyzer, two channel null depths over the above frequency band were measured. The filter to be matched was adjusted via three variable capacitors until a null depth in excess of 40 dB was achieved. In a few cases, the depth could only

be brought down to 37 or 38 dB. Without spending exorbitant amounts of time for this demonstration system, it was decided to accept those few matches below specification.

With all the IF hardware complete, a path length adjustment was implemented to insure all time delays to the mixers are equal. Care was exercised to insure that phase shifts were equalized by installing similar components in the channel sample path to those in the channel sum path. The final IF adjustment was done on a network analyzer with attempts to add cable lengths to the individual channel sample paths until $\frac{d\phi}{dw}$ was equal to the reference at band center. It was also noted what the absolute phase difference was after line-length equalization, and never exceeded 10°. This is a constant number across the board and can be completely removed in the following DC processing circuits as will be shown in the following section.

4.4 Baseband Processing and Control Circuits

The issue of control circuit bandwidth vs system nulling bandwidth was discussed briefly in Sec. 4.1. Looking at the nulling bandwidth of 10 MHz, the correlator and control must estimate correlation of signals in this bandwidth. Since a stable value for this quantity is desired, the bandwidth used for correlation must necessarily be significantly smaller than 10 MHz. From the available literature, a bandwidth reduction of 20 or greater has been used with success. Applying this concept here would put an upper limit of 500 kHz on the analog control closed loop response.

The lower frequency bandwidth is set by the residual time constant of low pass circuitry following the I and Q mixing to baseband. As this system was originally conceived as a frequency hopping scheme with a hop interval of 13.3 msec, it appeared that this was the best choice for the first order time constant also. This time, of course, is the interval required for the weight voltage to be within 1/e of the final value when they are relaxing to the pure noise condition. Stated another way, it is the approximate length of time required for the null placed on a jammer to decay away after the jammer has

been turned off. This translated to a minimum closed loop bandwidth of $f_o = 1/(2\pi\tau_o)$ or 12 Hz.

Combining the minimum and maximum control bandwidths and recalling that an increase in the largest system eigenvalue (roughly corresponding to a proportional increase in input power level) will increase the closed loop bandwidth one for one, the available dynamic range can be computed. Available dynamic range is 10 log [500 kHz/12 Hz] which equals 46 dB. As a minimum dynamic range of 40 dB is desired, this puts the highest closed loop design bandwidth at 120 kHz. This is the highest frequency to which the low frequency circuits must still perform as true first order filters. This implies phase shifts must be within a few degrees of 90° and amplitudes must follow a 1/f relationship at f = 120 kHz.

The above restraints plus the high DC gain forced the choice of high speed op-amps and careful selection of feedback components and layout. Referring to Fig. 4.2, the capacitor in the feedback circuit of the op-amp is approximately 0.22 uF. One problem in constructing the active (or passive for that matter) filter is that this capacitor must look capacitive for all frequencies up to 120 kHz. Further, it must look like the same value. If the dynamic range needed to be increased by another 10 dB, then the capacitor would have such a low impedance that lead length and residual series inductance could easily approach the magnitude. This is another component which must be considered in the overall design. Given that it is very difficult to analyze a system of N channels which have N different residual time constants, considerable effort was devoted to procuring and selecting the op-amp feedback resistor and capacitor pairs to be within 0.1% for all channels. This design specification was met, and all channels had identical responses as best could be determined.

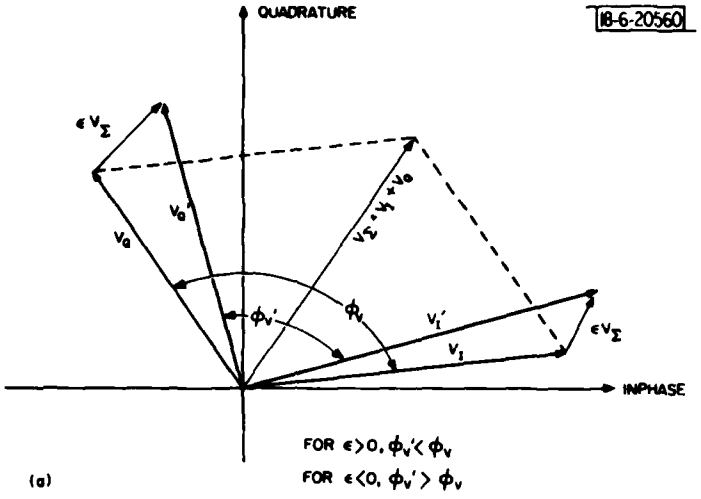
After all the IF hardware is specified and built, hybrids measured, line lengths equalized, and the active low pass circuits matched to each other, in general, there will still not be exactly 90° separation between the I and Q outputs following the low-pass filter. Also if the weights are set up for

W_I = 1v and W_Q = 0v, in general, the V_Q will not be exactly zero, implying an absolute rotation of the vectors in the I and Q space. Figure 4.3 (a) illustrates the method used to adjust the V_I and V_Q to achieve a new set of vector V_I' and V_Q' which are spaced 90° apart. The implementation used to generate the signal summation signal (V_{out}) is shown in Fig. 4.4 (a). Figure 4.5 illustrates this in the hardware built and also shows adjustments to make $|V_I'| = |V_Q'|$. Figure 4.3 (b), on the other hand, shows how the pair of vectors is rotated conceptually to preserve the 90° separation as well as the equal magnitude. Figure 4.4 (b) is a simplified schematic of two circuits which could generate $\Delta V_I'$ and $-\Delta V_Q'$. These work only as long as the potentiometer can be adjusted at the same time in the same way. Again referring to Fig. 4.5, this was implemented with a series of switches which, through a binary code, could quantize the value for Δ and thus make identical adjustments on the I and Q channel. With the values shown in Fig. 4.4, one can achieve a ± 14° adjustment on the 90°-ness of V_I and V_Q and a ± 27° absolute rotation of V_I' and V_Q' vectors with a quantization of 0.45°.

As alluded to earlier, if these fixed phase differences and offsets are not too large, the first order system will still work, as most functions are affected by terms like cosine of the phase error. This would say that 10° to 15° of offset as well as quadrature error would not hamper performance, but these adjustments were included so that this could be verified and larger phase errors, if they occurred, could be minimized.

After the baseband conditioning, the so-called steering vector (or voltage) inputs are inserted. These are simply DC voltages added directly to the final V_I'' and V_Q'' voltages to insert a preference pattern vector into the overall system. In order to save hardware, these are introduced into the system with a -1 multiplier (see Fig. 4.5). This is just a bookkeeping matter, as these voltages are simply programmed via a D/A.

The final portion of the subsystem consists of weight setting for initial conditions. In the frequency hopping application, it was desired to start



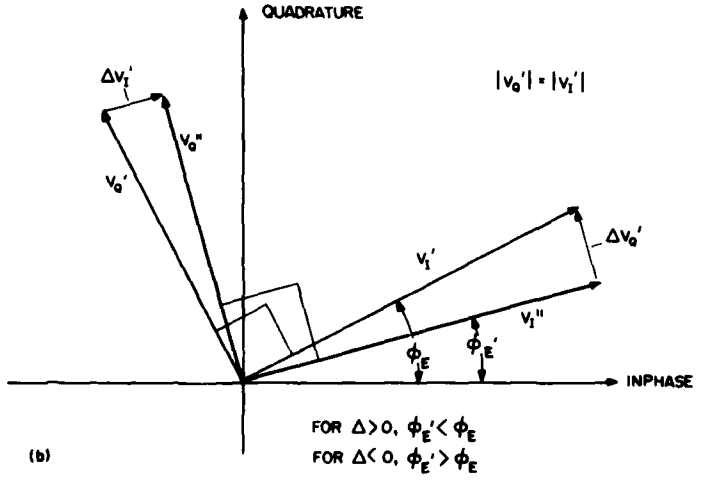


Fig. 4.3(a-b). (a) Method of adjusting relative phase between two vectors of approximately equal magnitude to achieve 90° separation. (b) Method of adjusting absolute phase of a pair of vectors to equal length while still maintaining the same 90° separation and equal amplitudes.

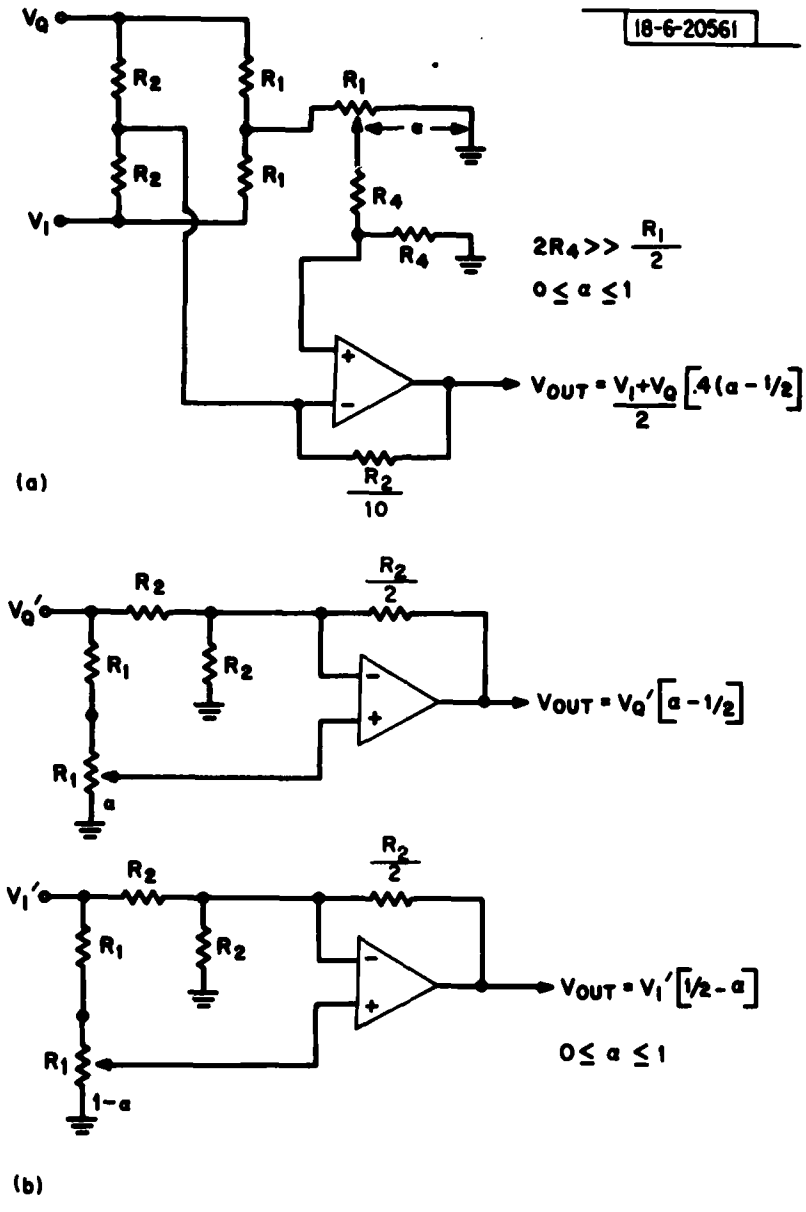


Fig. 4.4(a-b). (a) Circuit to adjust for 90° phase shift between I and Q output of baseband circuits. (b) Circuit to derive adjustments for absolute phase offset (vector pair rotation).

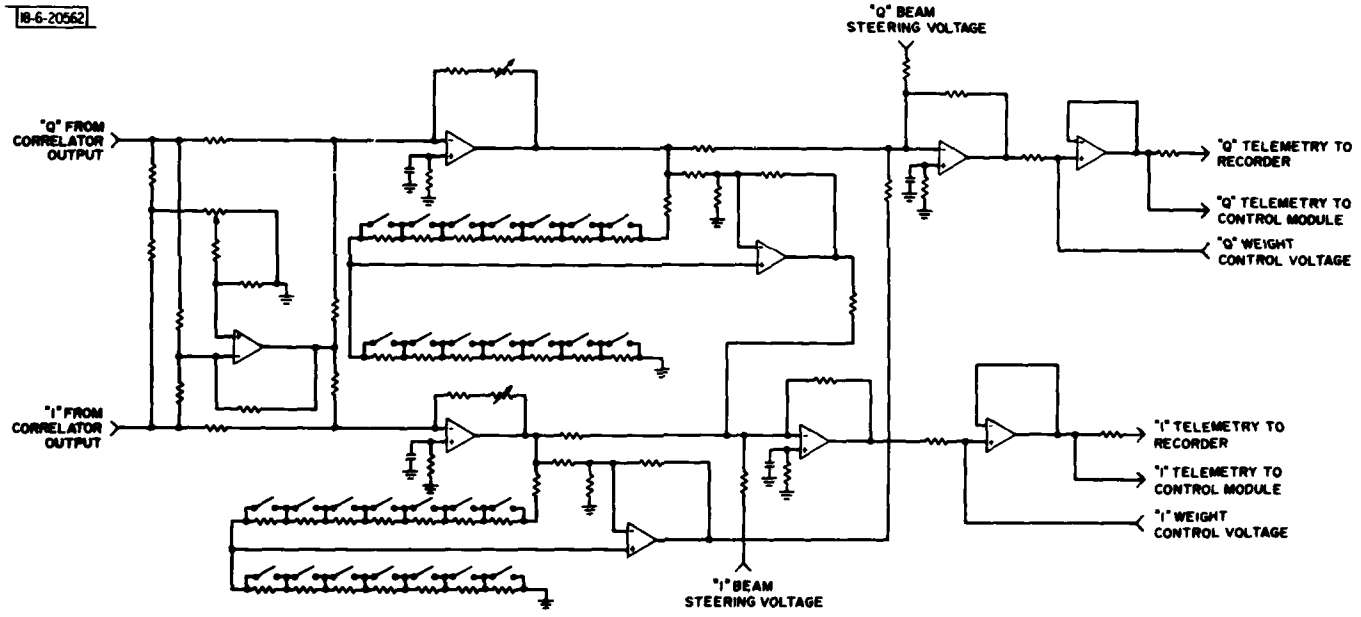


Fig. 4.5. Simplified schematic of the weight and conditioning board in the correlator module.

the weights adapting from the place they were the last time the system was in the particular frequency band. This implied a presetting of the weights which would set up the initial conditions of the low-pass filter reactive component. Figure 1.3 shows the overall interconnection scheme, whereas, Fig. 4.2 delineates the specific connection to the low-pass filter board. The source resistance feeding the weight initialize was picked so that in the closed loop the final weight voltage would slow to the correct output from any initial state within 300 μsec. At the end of 300 μsec the op-amp feedback capacitor would be charged to the appropriate value, the weight voltage would be correct, and the weight initialize line could be grounded. Due to the way in which the circuits were constructed, this causes no step transients in the system at the beginning of adaption.

4.5 Correlator Units and System Integration

The correlator units were constructed for interchangeability and flexibility. Each portion of hardware which was duplicated eight times was installed in a subassembly. These eight subassemblies, except for the sum signal amplification and splitting, are the heart of the correlation and control. Since they are identical, they could be tested in an identical fashion. In fact, the situation was such that they were computer tested with very little operator intervention. This greatly reduced the time required for testing and greatly increased the quality and quantity of data which was taken. Temperature gradients unit to unit were minimized by mounting these subassemblies on the same chassis as a vertical "slice". The single subassembly which contained all sum channel conditioning, the single function module (see Sec. VII), was installed vertically in the middle of the chassis with four correlator units on each side. This minimized cable matching and harness interconnection problems.

The single function module contained the capability for monitoring a number of quantities including wideband and narrowband sum channel power and all eight I and Q weight voltages. Through program control via another

interface, any of these quantities could be multiplexed into the system CMD/TLM unit (see Sec. 8.2). This unit has the capability of issuing commands to the correlation and control chassis via the single function module to change the data examined as explained above or actually manipulate system gain through the 2-bit attenuator described earlier. Upon final integration, this type of operation aids in overall system troubleshooting, provides system readiness assurance, and allows system testing to start from a known initial state.

Figures 4.6 (a) and (b) show the actual correlator module as it was fabricated and incorporated into the system. Eight identical units were built and installed.

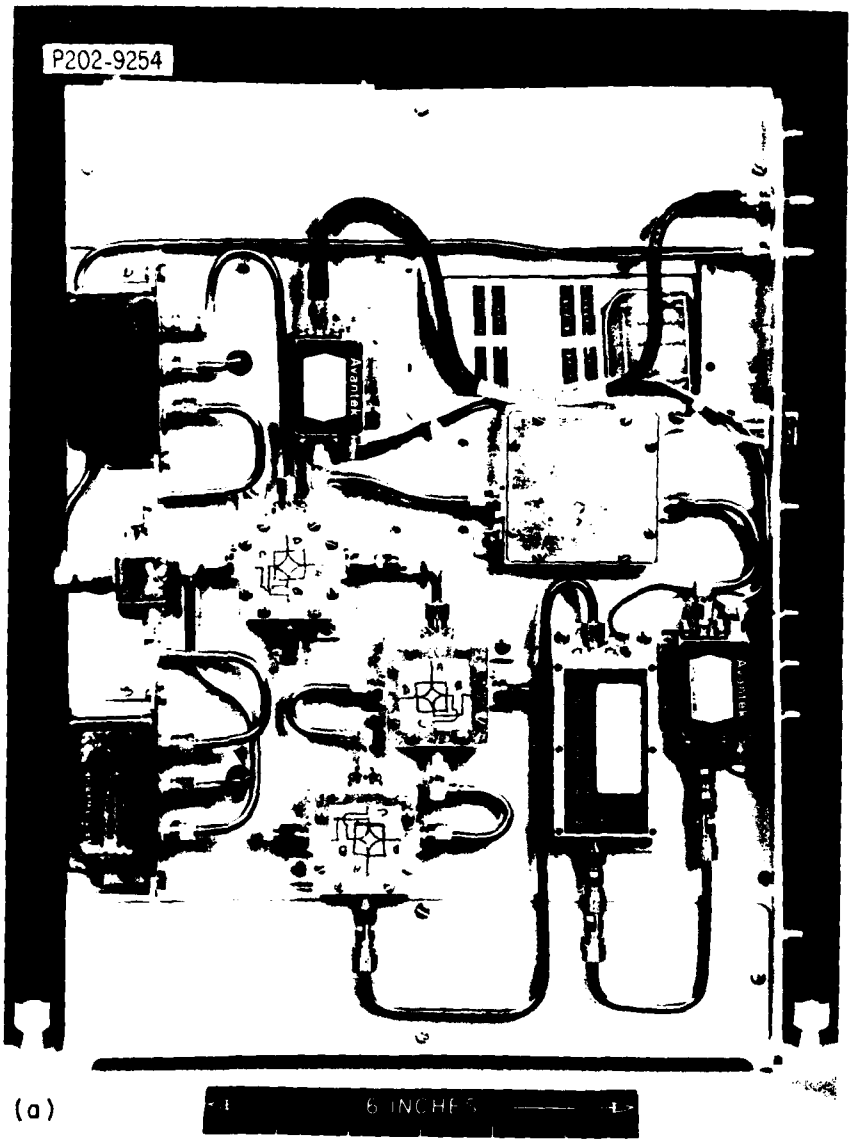


Fig. 4.6(a). Correlator module.

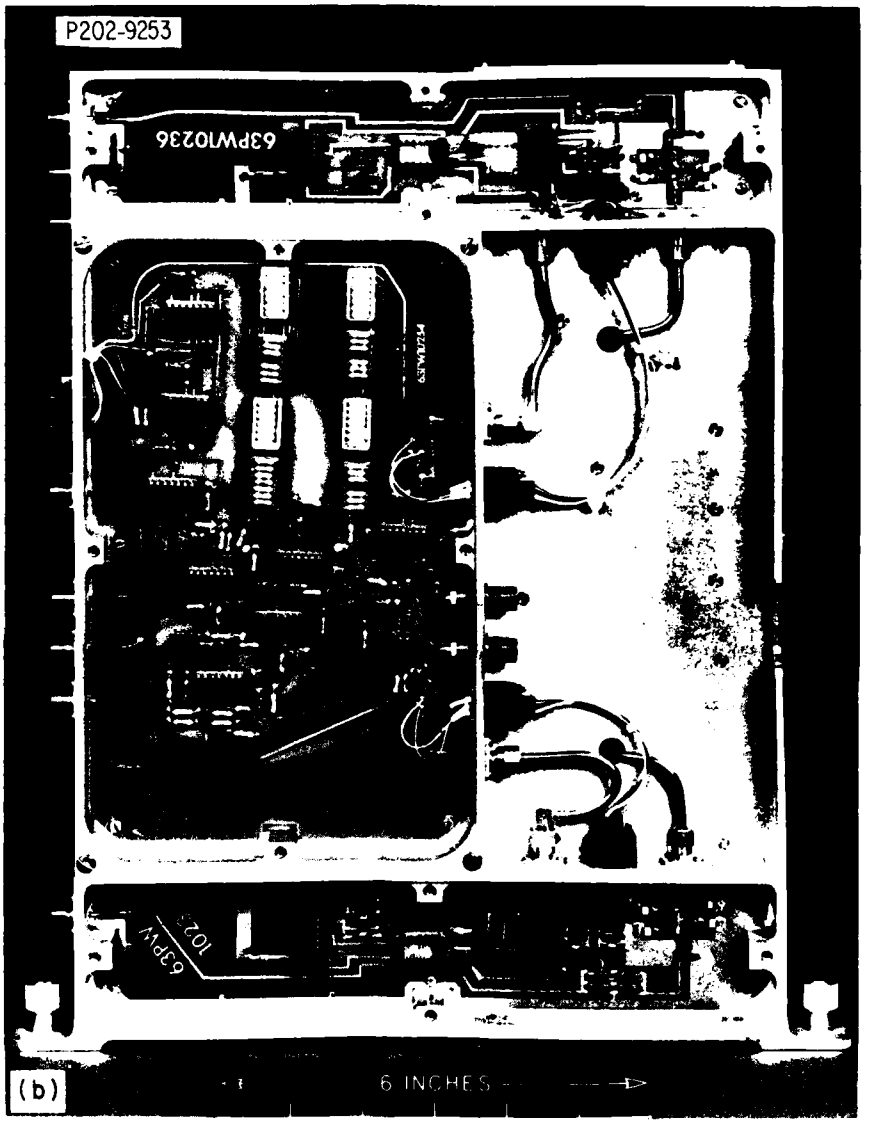


Fig. 4.6(b). Correlator module.

V. DIGITAL INTERFACE

5.1 Introduction

The digital interface between the analog feedback loops of the nulling antenna system and system test controller consists of two pieces of equipment, the Beam Steering Weight Storage and Timing Unit and the Interface Controller and Buffer Memory.

The Beam Steering Weight Storage and Timing Unit (BSWS&T) is a laboratory-built piece of hardware which functions as the direct control interface for the analog feedback loops. Beam steering voltages are provided to set the unadapted antenna pattern. Feedback loop weight voltages are A/D converted and stored at the end of each frequency hop for use in initialization when the same frequency is later repeated. Time of all events within the frequency hop interval is provided by this unit. Initialization of the feedback loops at the start of each hop interval is also controlled by this unit.

The Interface Controller and Buffer Memory, a PDP11/03 minicomputer, provide the interface between the BSWS&T and the IEEE-488 instrument bus operated by the test system controller. The PDP11/03 accepts commands and data from the IEEE-488 bus (Ref. 13) in the form of ASCII character strings and interfaces to the BSWS&T via a 16-bit parallel digital interface and a 16-bit parallel direct memory access (DMA) data interface. Binary control and data values are passed over the parallel interface. Measurements of feedback loop performance in the form of measured weight values and hop frequency segment numbers are stored in the PDP11/03 which acts as a data buffer and formatter. Following a measurement, stored data is formatted into ASCII character strings and passed at a lower rate to the test system controller via the IEEE-488 bus. Figure 5.1 shows the interface relation to the adjacent portions of the system. Sections 5.2 and 5.3 describe in more detail the digital portion of the BSWS&T unit and the software used in the PDP11/03. Section VI of this document describes the A/D and D/A portion of the BSWS&T unit.

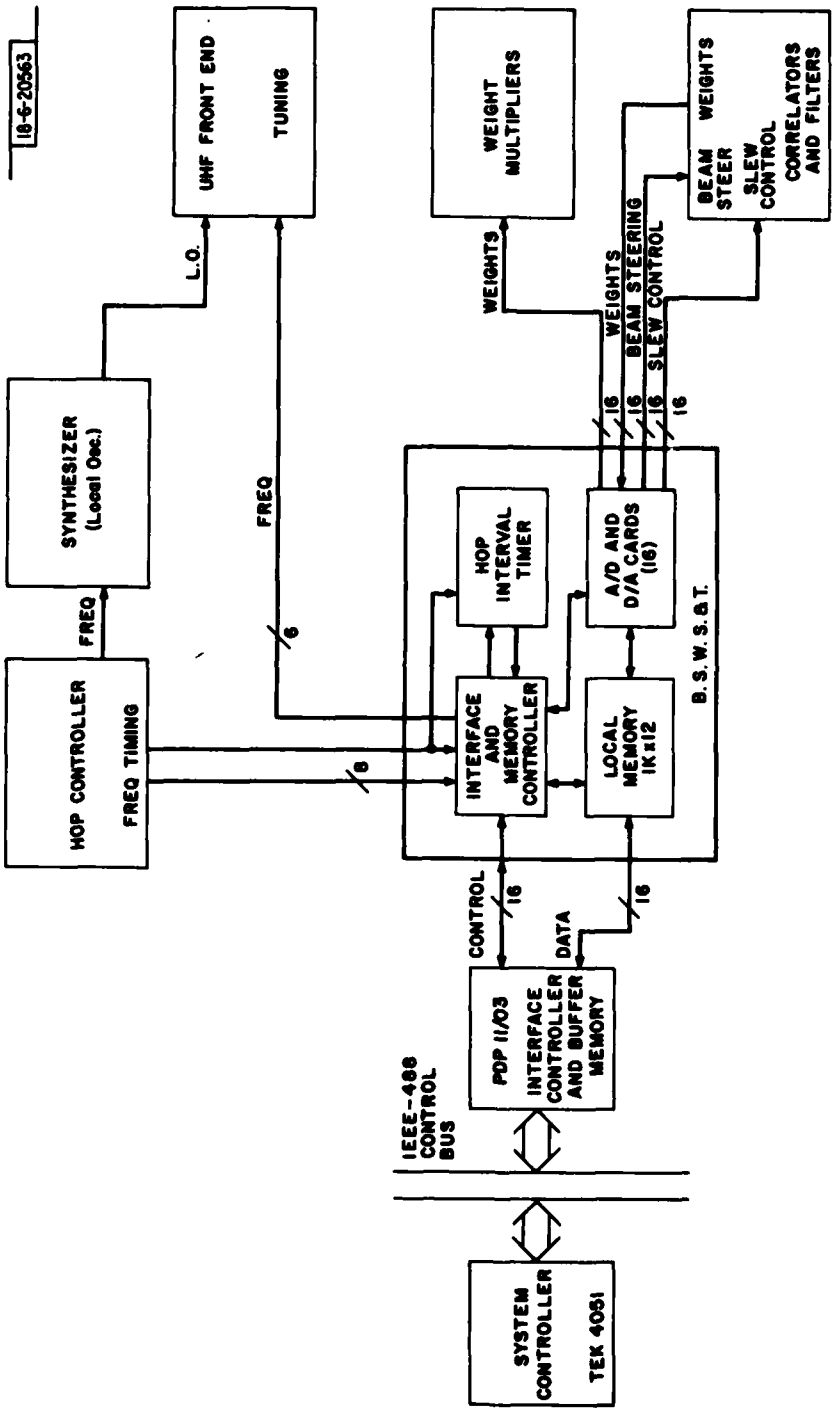


Fig. 5.1. System interface of BSW&T.

5.2 Digital Content of the BSWS&T Unit

The BSWS&T unit contains a memory, a memory and interface controller, a timer, and a set of 16 identical A/D-D/A boards. The memory has a 1024 × 12-bit capacity for storage of 32 sets of 16 weight values and 32 sets of 16 beam steering values. It is called the local memory to distinguish it from the buffer memory function of the PDP11/03. The memory and interface controller operates the local memory interface to the PDP11/03 direct memory access (DMA) channel and the interface to the A/D-D/A boards. The timer performs the generation of all event times within the hop interval and serves as a controller for activities performed within each hop. The A/D-D/A cards are described in Section VI. The local memory, memory controller, and timer are described in this section.

The BSWS&T is constructed as a 10-1/2 inch high rack-mount unit containing two card cages. The three logic cards (memory, memory controller, and timer) are contained in one cage. An adjacent cage contains the 16 A/D-D/A cards. All cards are interconnected with a wire-wrapped backplane. Analog connections to the A/D-D/A cards are at the opposite end of the cards from the backplane. All external connections to the BSWS&T unit are on the rear panel of the unit enclosure.

5.2.1 Local Memory

The local memory card contains a 1024 × 12-bit bipolar RAM configured as a dual port memory. One port, with separate input and output lines, is connected via flat ribbon cables to the DMA interface of the PDP11/03. The second port is a bi-directional data bus which interconnects all 16 A/D-D/A half-channel cards. The local memory is used to store 32 sets of beam steering vectors and 32 sets of weight values, corresponding to the 32 frequency segments of the hopping bandwidth. The vectors are 16 elements of 12 bits each. Functionally, the steering vectors are written only from the PDP11/03. Weight values may be written from either port, but are normally the values measured by the A/D converters on the half-channel cards.

5.2.2 Memory Controller

The local memory controller logic performs a variety of control and interface tasks. The principal function is control of the local memory. Since the local memory must pass information to and from both memory parts, the controller handles the interface handshaking for both sets of transfers. The basic control structure is a small micro-programmed state machine consisting of a state latch, a condition multiplexer, output strobe demultiplexers, and a microcode ROM. The controller is programmed to perform transfers to and from the channel cards on command from the main timer logic. Data is transferred at a rate of 5 words per μsec to the channel cards, and half that rate from the cards to the memory. A 16-bit parallel interface from the PDP11/03 is used to pass hop frequency selection information and some control information. The PDP11/03, through the parallel interface, may request transfer of data via the DMA channel under the control of the memory controller. There is also an absolute control mode in which the PDP11/03 may cause termination of all hop-related operation and request DMA data transfers. Each DMA transfer consists of one set of 16 words.

5.2.3 Timer

The main time logic determines the structure of events within the hop interval. Timing is started by a start-of-hop pulse from the hop controller. Events include generation of strobe pulses to the correlator to bracket initialization time, commands to the local memory controller to cause data transfers to and from the A/D-D/A cards and local memory, start of A/D conversions, and operation of loop initial mode select for the A/D-D/A cards. The resolution of events is 1 μsec. Event times are determined by the content of two sets of ROMS.

5.3 Interface Controller and Buffer Memory

The PDP11/03 processor with its software provides the control interface between the system test controller (via the IEEE-488 instrument bus interface) and the BSWS&T unit (via two parallel 16-bit interfaces). The overall function

provided is control command interpretation and execution, and data interface and buffering. To perform these functions, the software is partitioned into functional sections. The IEEE-bus software provides the detailed handling of the modified IBV11-A IEEE-bus interface card (within the PDP11/03) and implements all of the required bus interface functions in accordance with the specification requirements of IEEE-Std-488-1975. A main program performs command line recognition and calls appropriate functional subroutines to execute command requests. A set of subroutine and interrupt service routines provides the detailed interface interaction with the BSWS&T hardware. The software was written to operate as a single self-contained job in memory without additional computer peripherals. The only deviation from this was the use of the console CRT to provide visual indication of command execution.

5.3.1 Main Program

The main program consists of two sections. The first, an initialization section, is executed once at the start of the program to set interrupt vectors, initialize variables, and enable interrupts from the IEEE-bus interface. The second section is a continuous loop which calls subroutines for processing input commands and formatting output lines when indicated by a set of status bits. The status bits indicate the state of listen and talk buffers accessed from the main program and the need for generation of additional output lines.

The chief objective of the main program loop is to maintain continuous operation. All subroutines called from the main program must contain no infinite loops. They must return to the main loop in a finite time. Any functions which may not be completed in a finite time are split into sections which will execute in a finite time. Indefinite delays between sections are handled by monitoring status bits in the main loop. When conditions are satisfactory, a waiting section is executed as a subroutine from the main loop.

The subroutine to interpret and execute input command lines is given the highest priority in the main loop. As long as there are more input lines ready to process, the main loop continues to call the command line processing subroutine. When all input lines are finished, the status bits relating to talk function requests are checked. If there is more data to convert to output lines, and a talk buffer is available, a formatting routine is called to prepare the next output line. If there is no output data waiting to complete a commanded output exchange and the IEEE bus interface has suspended operation to wait for a filled talk buffer, a status response is initiated. The status response satisfies IEEE-bus talk requests for which no prior data request has been received.

5.3.2 IEEE-Bus Software

The IEEE-Bus software consists of a set of routines to interface between the main control program and the IEEE-Bus via the modified PDP11/03 IBV11-A interface card (Ref. 14). This collection of routines handles all interrupts from the IBV11-A interface and all direct access to the IBV11-A status and data registers. Functions provided are activation of bus operation, interpretation of all BUS command messages, maintenance of activity status (addressed modes, etc.) and management of input and output data buffers supplied by the Main Control Program during Listen and Talk operations.

Separate routines include:

1. BUS Initialization Subroutine which is called following power-on, establishes a starting state for BUS operation.

2. Listener Interrupt Service is entered when a command or data has been properly received from the BUS.

3. Talker Interrupt Service is entered when the BUS is ready to accept data.

4. Service Request Interrupt is entered when this system or other instrument requests service from the system controller.

5.3.3 Command Execution Subroutine

When the main program finds a status bit set indicating a filled input buffer, the command line subroutine (CMDLIN) is called to process the command. This subroutine first reads a two-character command mnemonic identifying the command. A table lookup of the mnemonic is performed. Tabled quantities include the mnemonic, the number of numeric arguments required, the address of an argument storage block, and the address of the individual subroutine to perform the command function. After extracting the required arguments from the input command line, the CMDLIN routine calls the appropriate command execution sub-routine. Control is not returned to the main program until the command execution subroutine has been completed.

Described below is the set of commands for control of the digital interface to the Nulling Antenna System. These commands communicated via the IEEE-488 bus provide the sole access between the Test System Controller and the Buffer/Local memory portion of the antenna system. Each command line consists of a two-character mnemonic followed by an optional set of number arguments. Numeric arguments are 1 to 4 digit unsigned decimal numbers. If numeric arguments are less than 4 digits in length they must each be followed by a non-numeric character serving as a delimiter. Leading zeros are included in the digit count. A nonnumeric delimiter character must be included after the mnemonic if there are numeric arguments. A listing of argument definitions follows the Buffer Commands section.

Buffer Commands

Take Control (TC) (no numeric arguments)

Assert absolute control and force synchronization of local memory controller regardless of previous state. This command is used when the previous history (and hence current state) is either unknown or unimportant. All measurement controls are set to a non-active state.

Write Vector (WV, frequency, vector)

Deliver 16 data words to a specific frequency location in the local memory. Distinction between steering vectors and weights is included as part of a single numeric frequency value (0-63 for steering vectors, 64-127 for weights). This command is usable only when the nuller is not running (HALT mode).

Read Vector (RV, frequency)

Read 16 data words from a specific frequency location in the local memory. The frequency specification is the same as used in the Write Vector command. This command is for use in the HALT mode.

Start Operation (SO, wfn, trig)

This command will start operation (RUN mode) if the system was previously in HALT mode. If the system is already in RUN mode, no action is taken. No data gathering will take place when operation is started with this command. An argument specifies the weight freeze* channel selection. The trigger option will set the device trigger function to complete the start operation to facilitate coordination with other IEEE bus operations.

Start Measurement (SM, wfn, trig, mode, first block, no. of blocks)

The start measurement command will simultaneously start operation and measurement (acquisition of weight vectors) if the system was in HALT mode. If the system was in RUN mode, only the measurement is started. If this command is issued

*This is the channel(s) not allowed to adapt, held at its initialization value.

in RUN mode any active measurement may be disrupted. Arguments to weight freeze channel select and measurement type are included. The weight freeze argument value will be ignored if already in RUN mode.

Measurement options include buffer use (single pass or circular), start and length indices for buffer use, and measurement rate (one or ten samples per hop). A device trigger option may be used for coordinated start in single pass or coordinated stop in circular mode.

Terminate Measurement (TM) (no arguments)

Any measurement in operation is terminated. This command is to be used to terminate circular mode measurements. Details of where the measurement stopped have not been clearly defined. The operation of the nuller (RUN state) is not disturbed.

Terminate Operation (TO) (no arguments)

Both measurement and operation are terminated. The measurement will be allowed to continue through the timeout of the hop interval timer. The system is left in the HALT mode.

Read Memory (RM, first block, number of blocks)

Read data from the buffer memory. Arguments include starting block and number of blocks to be read. Each block consists of a frequency number and sixteen data values. The buffer memory is operated as a circular structure. This command may be used in either RUN or HALT modes. Use of this command while a measurement is active should be avoided.

Initialize Channels (IC, frequency)

Moves the local memory content for the argument frequency to the channel cards and forces card initialization. The RF frequency control is also set correctly.

Argument Definitions

Frequency:

A numeric value in the range Ø through 127 indicating the RF frequency designation.

Vectors:

16 numeric values in the order 1I through 8Q. The range is Ø (+2.5 volts) through 4095 (-2.5 volts). The vectors may be either steering vectors or weight vectors.

wfn:

Weight freeze number indicating the channel which will not be allowed to adapt. A value of Ø means all channels are frozen. Values 1 through 8 select channels 1 through 8. A value of 15 leaves all channels unfrozen.

trig:

Trigger unable. A value of Ø indicates immediate command completion. A non-zero value leaves final execution of the command for receipt of a device trigger command.

mode:

Data acquisition mode:

0 for one sample per hop, fill buffer and stop
1 for ten samples per hop, fill buffer and stop
2 for one sample per hop, fill buffer circularly
3 for ten samples per hop, fill buffer circularly.

first block;

A number in the range ∅ through 989 indicating the first data buffer block to be used for data storage or retrieval.

No. of blocks:

The number of blocks of data (one 16 word vector per block)

VI. A/D, D/A INTERFACE CIRCUITS

An integral portion of the Beam Steering, Weight Storage and Timing Unit (A2) consists of digital-to-analog (D/A) and analog-to-digital (A/D) converters with assicated hardware (Fig. 6.1) for the purpose of interfacing with the Weight and Summer Network (A13) and the Correlation and Control unit (A7). Sixteen identical printed circuit boards were used, one each for the I and Q portion of the eight channels in the system. Figure 6.2 shows a block diagram of a single half-channel (I or Q) interface card.

In the normal sequence of events, the interface cards accept weight vectors and beam steer vectors from the timing and control memory and return adapted weight values from the correlators to the memory via the 12-bit bi-directional bus. On an individual card basis, the weight D/A output goes to a solid state switch (SW1) which allows this output to connect directly with the Weight and Summer Network during the 300 μsec initialization period of each hop (position 1). The D/A output also goes to a comparator followed by another solid state switch (SW2) which forces the A7 weight control voltage to slew to the desired value during the initialization period (position 1) (see Sec. 6.4). The beam steer D/A output goes through a unit gain buffer amplifier which delivers the beam steer value to the correlators. During the normal adapt period of the hop interval, SW1 is in position 2, which closes the adaption loop (see Fig. 1.3) and lets the weight control voltage (A7) feed the weight (A13) directly. SW2 is also now in position 2 which allows the A7 loop to adapt. Near the end of the hop, the A7 weight control voltage is sampled and held (S/H) and converted by the 12-bit A/D. This digital value is then transferred to the timing and control memory and stored in the bin associated with the particular hop frequency.

The interface cards can be operated in several other modes for testing and test purposes. Under controller command, SW1 can be kept in position 1 during the entire hop, thus allowing a channel (both I and Q) to be used as a reference channel. As one method of viewing the weight control voltage

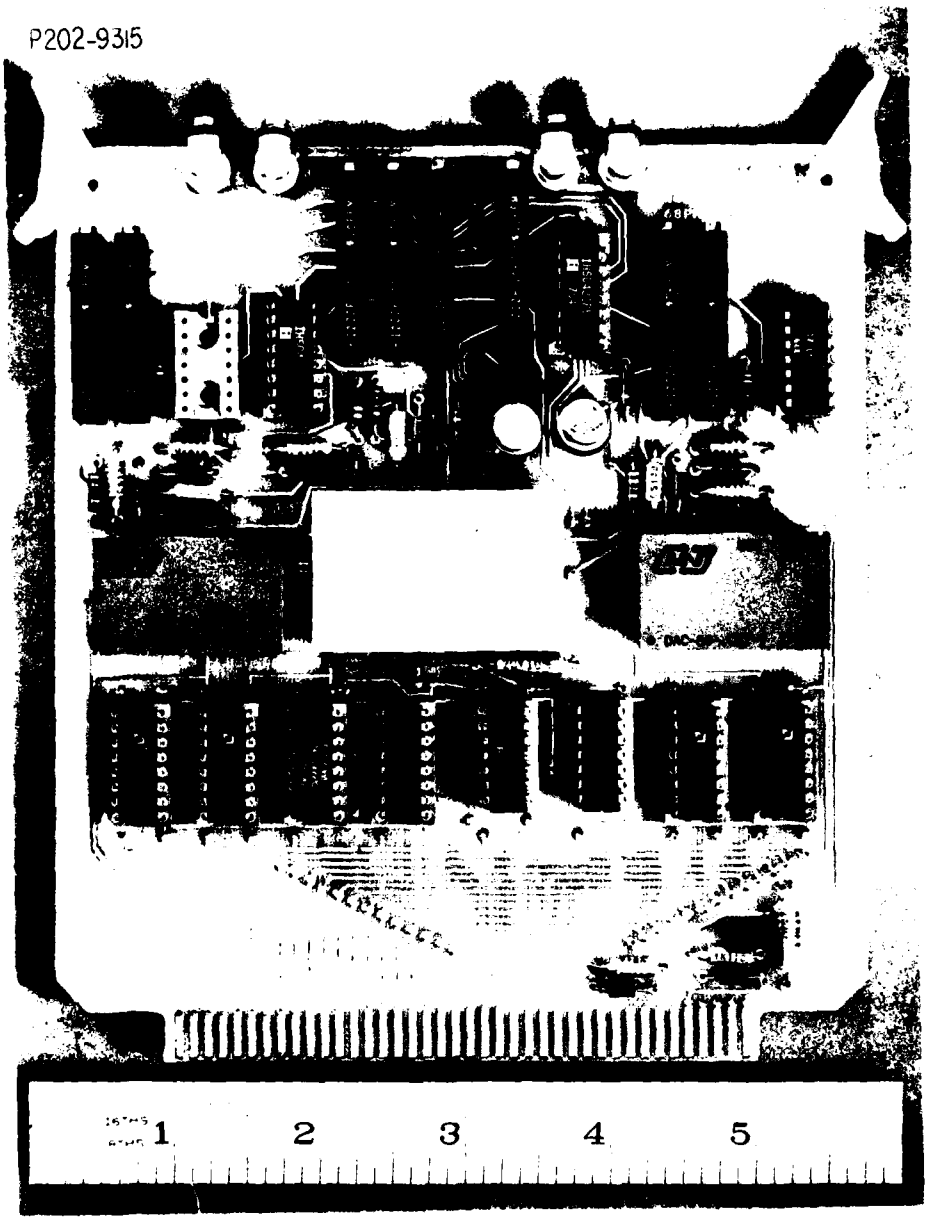


Fig. 6.1. Beam steering, weight storage, and timing unit (A2) A/D, D/A board.

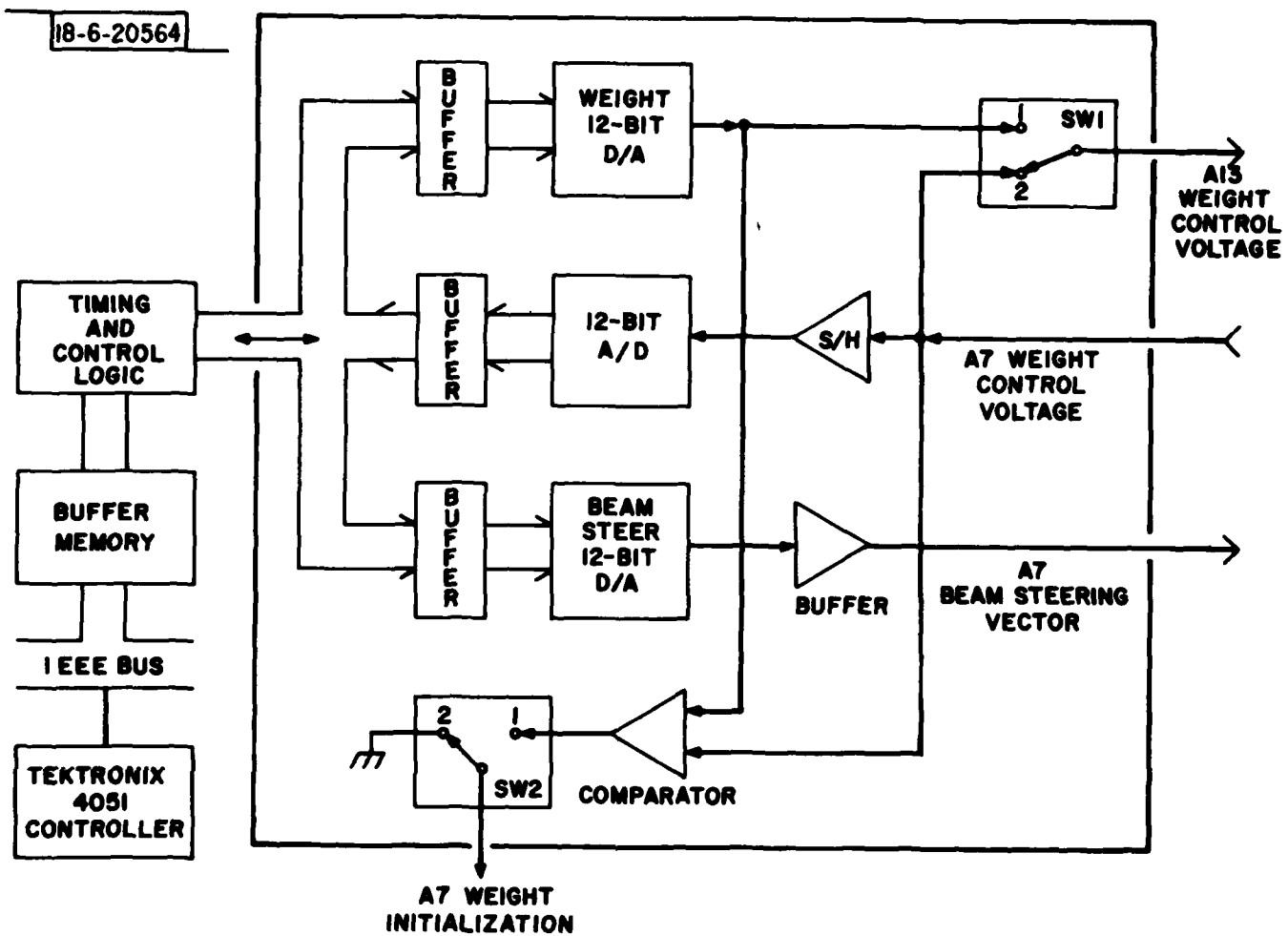


Fig. 6.2. Block diagram A/D-D/A interface circuit.

adaption, under controller command, the input weight control voltages can be sampled during the hop interval and the values transferred and stored in memory for latter display. To facilitate board integrity checks, with a card disconnected from the bus, the circuitry can be configured such that an analog signal into the A7 weight control voltage input port can be sampled, A/D converted, and D/A converted. The weight and beam steer D/A outputs can then be compared to the analog input.

All components on the interface card are standard commercial items; the A/Ds and D/As were chosen for their relatively small size. The units perform the conversions faster than is required, but the circuits were originally designed and fabricated when the overall nulling system was scaled to L-band. With 12 binary bits, the A/Ds and D/As have a decimal counting range from 0 to 4095 which corresponds to a +2.5 volts to -2.5 volts voltage range respectively.

VII. SINGLE FUNCTION CIRCUITS

The single function circuits (Fig. 7.1) are part of the correlation and weight control unit (A7) (see Sec. IV). The circuitry is physically located in the center module of the A7 unit and provides support for the eight correlator modules in this unit through DC power distribution, commanding, and telemetry functions.

The DC power distribution involves 4 rows of five turret-type solder posts connected together for ground, +5 VDC, and ± 15 VDC. The three voltages and ground are received via a connector on the rear panel and are fanned out from the solder post to each correlator. No conditioning of any kind is done to the DC power lines in this module.

There are four command lines from the command and telemetry unit (A1) which are used to operate a digitally controlled step attenuator in A7. Two of the command lines (A and B) are used to select one of the four possible settings of the attenuator while the other two command lines (C and D) are used to control the conditions under which the attenuator changes settings. The four values of attenuation are 0, 5, 10, 15 dB; Table 7.1 shows the relationship between the command lines and attenuator setting.

TABLE 7.1

COMMAND LINE VS ATTENUATOR SETTING

Command Lines		Attenuator Setting
B	A	
0	0	0 dB
0	1	5 dB
1	0	10 dB
1	1	15 dB

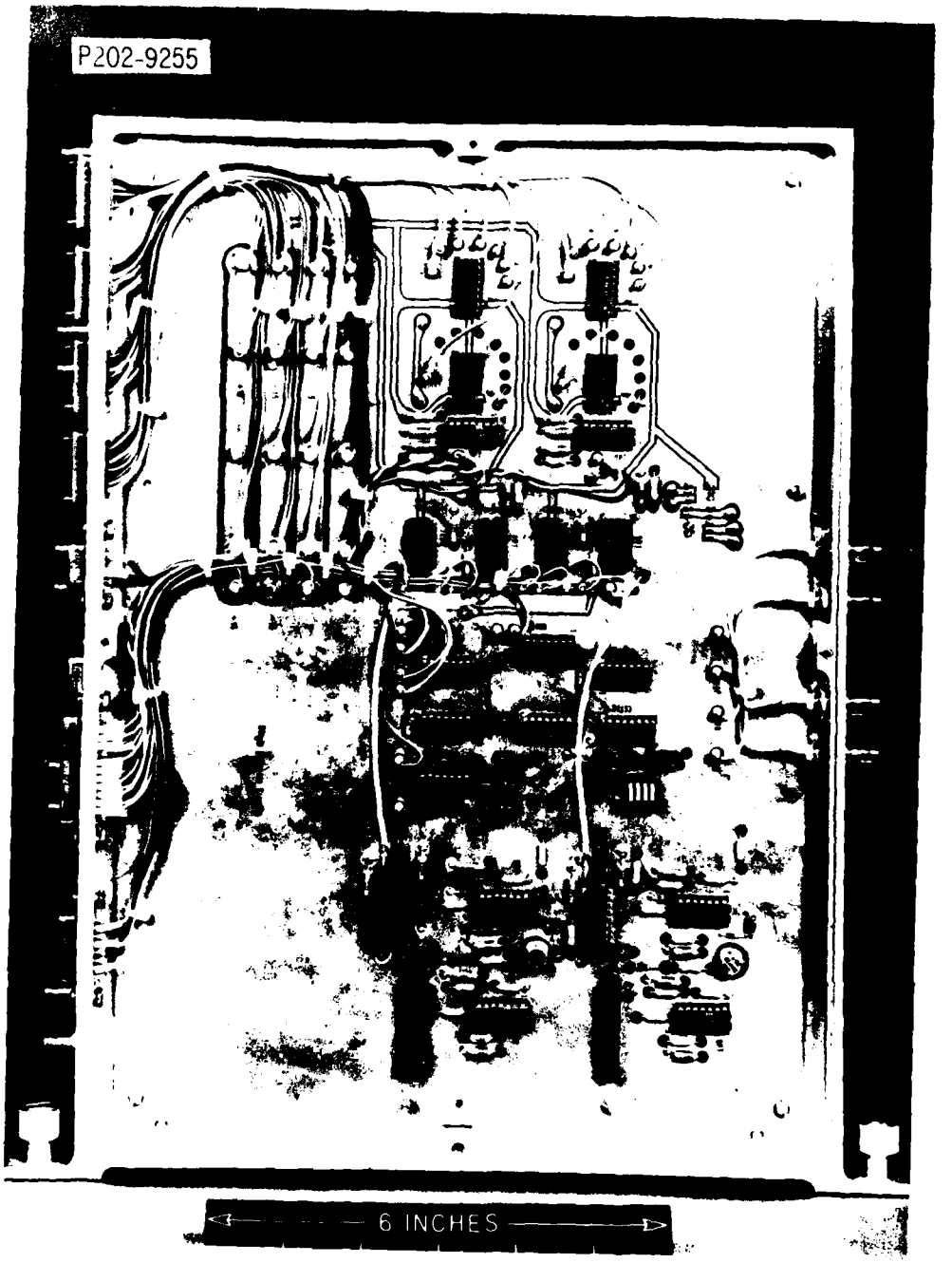


Fig. 7.1. Single function circuits board.

Command lines D and C provide four possible modes by which the set lines are allowed to control the attenuator; Table 7.2 shows this relationship.

TABLE 7.2

COMMAND LINES VS ATTENUATOR SETTING CHANGE

Command Lines		Attenuator Setting Change
D	C	
0	0	Immediately
0	1	On a logic 0 → 1 transition of the frequency hop pulse.
1	0	On a logic 0 → 1 transition of the beginning of adaption pulse.
1	1	On the logic 0 → 1 transition of either the hop or adaption pulse, whichever comes first.

For test purposes, switches can be inserted on the board to bypass the 4 command lines and manually control the functions.

The telemetry functions consist of two sets of analog multiplexers (one each for I and Q) whose inputs are various test points in the correlation and weight control units. Each set of multiplexers has four telemetry request lines which provide 16 possible telemetry points per set. Of the total of 32 maximum test inputs, only 18 are used in the system. The test points include 16 weight control voltages, one each for the 8 I and Q channels, and two system total output power level monitor points, one for the power in a 50 MHz bandwidth (wideband) and one for power in a 2 MHz bandwidth (narrow-band) about the carrier (hop) frequency. Only two analog telemetry lines, one from each set of multiplexers, can be selected for processing by the command and telemetry unit. If all points are to be looked at, then a sequence of telemetry requests must be sent. The 18 points monitored are divided with 9

per set, 8 weight control voltages and 1 power level per set. An address enable line (logic 1 enabled) is also provided by the command and telemetry unit. When A7 is not addressed, the multiplexers default to address 0 which selects the two power level monitor points. Table 7.3 which applies to both sets of multiplexers, shows the relation between the telemetry request (multiplexer address lines) and the selection of the 18 telemetry points.

TABLE 7.3

TELEMETRY REQUEST VS CONTROL LINES

Selected Telemetry	Enable	Telemetry Request Word MSB			LSB
Power Level	0	X	X	X	X
Power Level	1	0	0	0	0
Channel 1 Weight Control Voltage	1	0	0	0	1
Channel 2 Weight Control Voltage	1	0	0	1	0
Channel 3 Weight Control Voltage	1	0	0	1	1
Channel 4 Weight Control Voltage	1	0	1	0	0
Channel 5 Weight Control Voltage	1	0	1	0	1
Channel 6 Weight Control Voltage	1	0	1	1	0
Channel 7 Weight Control Voltage	1	0	1	1	1
Channel 8 Weight Control Voltage	1	1	0	0	0

(X indicates a "don't care" state)

The single function circuits board contains two logarithmic amplifiers which provide the necessary amplification for the narrow and wide-band power level detector signals. The outputs of these amplifiers are the actual telemetry lines which can be monitored. These same signals are also buffered and routed to the front panel of A7 unit for constant monitoring, if desired.

VIII. SYSTEM CONTROL AND INSTRUMENTATION

8.1 Control Programs

The control of the nulling system is handled by a Tektronix 4051 Graphics System microcomputer. Through a variety of programs, the 4051 can command the Beam Steering Weight Storage and Timing unit (A2) through the PDP 11/03, as well as the Correlation and Control Unit (A7), the Weight and Summer Network (A13), and the Hop Controller (A77) through the Telemetry and Control Unit (A1).

The 4051 system consists of a CRT, keyboard, and internal magnetic tape drive for program and data storage (See Fig. 1.2). The system connects to the General Purpose Interface Bus (GPIB) which is 8 bits wide, bit-parallel, byte serial, and in accordance with the IEEE-488 bus interface standard (Ref. 13). All programs are written in BASIC programming language. Refer to Ref. 15 for additional technical information on the Tektronix 4051 use and programming.

The major software support for the nulling system control consists of the following 5 programs:

1. The PDP 11/03 Interface Program
2. The PDP 11/03 Memory Data Plot Program
3. The A13 Transfer Switch Commanding Program
4. The Automatic Telemetry Program
5. The Telemetry and Command Exercise Test Program

A detailed description is shown below.*

8.1.1 The PDP 11/03 Interface Program

The PDP 11/03 interface program allows the user a variety of options through the selection of the user definable keys on the 4051 keyboard. These options include the ability to

a. send commands

b. receive and display data

*...shown do not necessarily reflect actual operating conditions of the ... included to show the program capabilities and formats.

c. write beam steering and weight control vectors directly in volts

d. send one of several pre-defined sets of vectors

e. send a sequence of commands automatically and/or repetitively

f. read and display the contents of the A2 local and buffer memories

g. re-run a program

h. load one of the programs 2, 3, or 4.

The examples below illustrate some of the most common user interactions with the PDP11/03 Interface Program. See Sec. V for explanation of commands and abbreviations. Arrows in the left margin indicate user inputs.

The following is an example of writing a vector:

```
HIT USER-DEF KEY #1 TO SEND A COMMAND
HIT USER-DEF KEY #2 TO PRINT A RECEIVED STRING
HIT USER-DEF KEY #3 TO SEND A WV IN VOLTS
HIT USER-DEF KEY #4 TO SEND SO,TO,RV
HIT USER-DEF KEY #5 TO SEND A RM AND PLOT
HIT USER-DEF KEY #6 TO SEND KEY 16,N&Y,SO 15 0
HIT USER-DEF KEY #7 TO SEND KEY 12,N&Y,SO 2 0
HIT USER-DEF KEY #8 TO RUN THIS PROGRAM AGAIN
HIT USER-DEF KEY #9 TO RUN TELEMETRY PROG FOR A7,A13
HIT USER-DEF KEY #10 TO RUN TRANSFER SWITCH PROGRAM
TO SEND ONLY RM WHEN NO PLOT IS DESIRED HIT KEY #1
HIT USER-DEF KEYS #11-18 TO SEND SPECIFIED WV'S IN VOLTS
HIT USER-DEF KEY #19 TO SEND A WV AND IC
HIT USER-DEF KEY #20 TO SEND WV 1,0,0,0,0,0,...

ENTER FREQUENCY
(1)→ 25
ENTER 16 ELEMENT VECTOR SEPARATED BY COMMAS (IN VOLTS)
(2)→ 1,0,1,0,1,0,1,0,1,0,1,0,1,0,1,0
DO YOU WANT TO SEND WRITE VECTOR AS IS?
(3)→ N
STRING HAS BEEN SENT
IC HAS BEEN SENT
```

The number 25 at input 1 refers to the 25th of the 64 hop frequencies. The string of numbers at input 2 is organized as channels 1I, 1Q, 2I, 2Q,...8I, 8Q. The N (no) response at input 3 causes the addition of the previously measured and stored system offsets to be added channel by channel to the vector at input 2. A Y (yes) response would have caused the vector at input 2 to be sent as is.

The following is an example of the system being allowed to adapt followed by the reading of the contents of a weight vector (after adaption) stored in the PDP11/03 memory:

```
SO 15 0 <--①
STRING HAS BEEN SENT
ENTER STRING TO BE SENT TO 11-03
TO<----------②
STRING HAS BEEN SENT
ENTER STRING TO BE SENT TO 11-03
RV 89<----------③
STRING HAS BEEN SENT
1,089,1983,1834,1903,1970,2104,2129,0899,2414,1956,2268,1967,1720,2102,1
935,2155,3917
FREQUENCY = 89       16 ELEMENT ARRAY:
 +0.0788  +0.1764  -0.0690  +1.4023  +0.1117  +0.0983  -0.0665  -0.1313
 +0.2607  +0.0946  -0.0995  -0.4475  -0.2692  +0.3999  +0.1374  -2.2827

0,064,0345

STATUS
```

Input 1 causes the system to start the adaption process while input 2 terminates the adaption and stores away the adapted weight values. Input 3 requests the reading of the weight vector for the 25th frequency in the hop band (recall from Sec. V that addresses 0 to 63 are reserved for beam steering vectors while address 64 to 127, beam steer + 64, are reserved for weight vectors). The next line of numbers begins with a status bit indicating a read vector (RV), followed by the weight vector address, followed by the weight values in raw counts out of the 12-bit A/D (refer to Sec. VI) in the order channel 1I, 1Q, through 8I, 8Q. These same values are then redisplayed, only written in volts. The last two lines indicate that the buffer memory has been cleared.

The following is an example of a pre-defined write vector:

```
DO YOU WANT TO SEND WRITE VECTOR AS IS?
Y
STRING HAS BEEN SENT
DO YOU WANT TO SEND WRITE VECTOR AS IS?
Y
STRING HAS BEEN SENT
```

The pre-defined user key takes care of sending the address number, vector values and channel initialization command. The user responses provide for offset addition if desired for the beam steer and weight vector inputs 1 and 2 respectively.

The following is an example of a user session to sample the weight control voltages during adaption:

```
DO YOU WANT TO SEND WRITE VECTOR AS IS?
Y
STRING HAS BEEN SENT
DO YOU WANT TO SEND WRITE VECTOR AS IS?
Y
STRING HAS BEEN SENT
ENTER STRING TO BE SENT TO 11-03
SM 15 0 1 0 50
STRING HAS BEEN SENT
ENTER STRING TO BE SENT TO 11-03
TO
STRING HAS BEEN SENT
0,064,0345

STATUS
ENTER RM ARGUMENTS (1ST BLOCK, NO. OF BLOCKS)
0 30
```

```
ENTER STRING TO BE SENT TO 11-03
RM 0,5
STRING HAS BEEN SENT
2,089,2012,1819,1949,1979,2045,2134,1162,2442,1948,2268,1953,1732,2094,1
939,2113,3826
FREQUENCY = 89       16 ELEMENT ARRAY:
 +0.0433  +0.1203  +0.0031  +0.0812  +0.1215  +0.1154  -0.0568  -0.0800
 +0.2790  +0.0836  -0.1056  -0.4817  -0.2692  +0.3852  +0.1325  -0.1716

2,089,2012,1818,1949,1978,2045,2134,1162,2442,1948,2268,1952,1732,2094,1
939,2118,3837
FREQUENCY = 89       16 ELEMENT ARRAY:
 +0.0433  +0.1203  +0.0031  +0.0812  +0.1215  +0.1166  -0.0568  -0.0861
 +0.2802  +0.0849  -0.1056  -0.4817  -0.2692  +0.3852  +0.1325  -0.1858

2,089,1947,1807,1977,2110,2015,1935,1151,2559,1967,2312,1867,1783,2086,1
965,1303,2191
FREQUENCY = 89       16 ELEMENT ARRAY:
 +0.1227  +0.0861  +0.0397  +0.0946  +0.0983  +0.2204  -0.0470  +0.9090
 +0.2937  -0.0763  +0.1374  -0.6245  -0.3254  +0.3238  +0.1007  -0.1752

2,089,1956,1811,1975,2099,2024,1959,1159,2544,1969,2309,1874,1781,2087,1
964,1390,2368
FREQUENCY = 89       16 ELEMENT ARRAY:
 +0.1117  +0.0885  +0.0287  +0.0849  +0.0958  +0.2118  -0.0482  +0.8028
 +0.2888  -0.0629  +0.1081  -0.6062  -0.3193  +0.3254  +0.1020  -0.3913

FREQUENCY = 89       16 ELEMENT ARRAY:
 +0.0983  +0.0946  +0.0238  +0.0934  +0.0995  +0.1960  -0.0519  +0.6258
 +0.2863  -0.0336  +0.0653  -0.5684  -0.3071  +0.3388  +0.1068  -0.7503

2,089,1972,1813,1868,2064,2030,2009,1147,2502,1964,2296,1893,1766,2091,1
958,1595,2788

FREQUENCY = 89       16 ELEMENT ARRAY:
 +0.0922  +0.0971  +0.0214  +0.0995  +0.1020  +0.1086  -0.0531  +0.5525
 +0.2863  -0.0201  -0.0470  -0.5549  -0.3034  +0.3437  +0.1093  -0.9042

0,064,0345

STATUS
```

Inputs 1 and 2 cause transfer of a pre-defined set of vectors to the PDP11/03 and initialization of the channels. Input 3 starts the measurement with sample to be taken and stored in a specified memory block, while input 4 terminates the measurement. The PDP11/03 output transfer buffers are then checked to insure they are empty, followed by input 5 which requests a block of memory ready for transfer to the 4051. Input 6 causes the desired portion of the requested block to be displayed in tabular form.

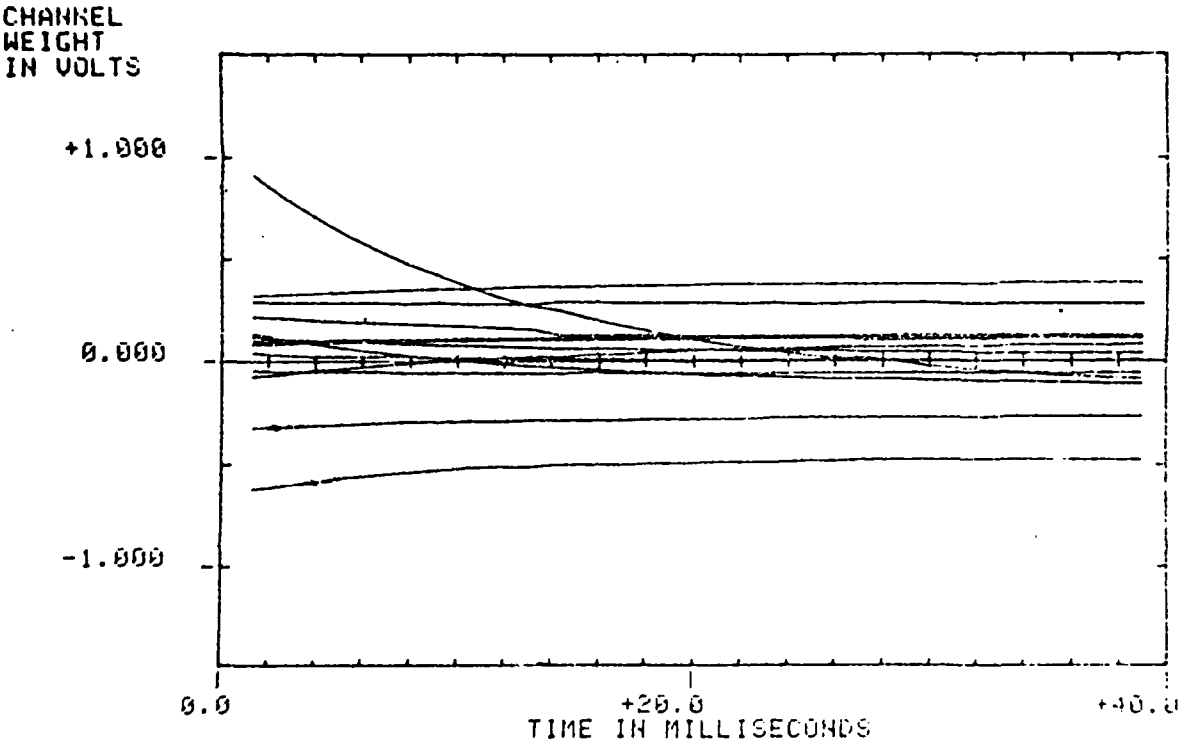
8.1.2 The PDP11/03 Memory Data Plot Program

In the PDP11/03 memory data plot program, following a read memory session, the user specifies a section of memory from which data is to be extracted and whether the data should be plotted for a particular channel, as a sequence of plots of all the channels (i.e. 1I through 8Q), or all 16 channels superimposed on one plot. The program labels the ones as time in msec versus channel weight voltage in volts. The user definable keys allow programs 1, 3, and 4 to be run from this program.

The following is an example of 16 channels on one plot:

```
ENTER LINE OF IDENTIFICATION FOR PLOT
(1,0) ALL CHANNELS, NO OFFSETS
TYPE 1 TO PLOT GRAPHS 1I,1Q,...,8I,8Q SEQUENTIALLY
TYPE 2 TO SELECT A CHANNEL TO BE PLOTTED
TYPE 3 TO PLOT ALL 16 GRAPHS ON ONE SCALE
3
```

(1,0) ALL CHANNELS, NO OFFSETS
ALL CHANNELS



8.1.3 The A13 Transfer Switch Commanding Program

The A13 transfer switch commanding program sets the 8 transfer switches on the Weight and Summer Network (A13). Refer to Sec. III. The user inputs a string of 8 "1"s and "0"s where a "1" turns the channel in that position ON and a "0" turns the channel in that position OFF. This program can load and run the PDP11/03 interface program, the automatic telemetry program, or re-run itself.

The following is an example of the transfer switch program:

```
CMD FOR BOX 1 (WEIGHT AND SUM)
ENTER AN 8-DIGIT BINARY NUMBER (1'S FOR CHANNELS ON
AND 0'S FOR CHANNELS OFF, I.E., 10100101)
10101010
```

In the example, the user input line causes channels 1, 3, 5, and 7 to be turned ON while channels 2, 4, 6, and 8 are turned OFF.

8.1.4 The Automatic Telemetry Program

The automatic telemetry program receives and displays telemetry data from the Correlation and Control Circuit (A7) or the Weight and Summer Network (A13). The user enters a number associated with each unit and the program runs automatically. After the telemetry has been displayed, the user has the option of storing the values on tape for later use. This program can load and run the PDP11/03 interface program, the transfer switch commanding program, or re-run itself.

The following is an example of the telemetry program for A7:

```
TELEMETRY PROGRAM
TYPE 1 FOR BOX A7, 2 FOR BOX A13
(1)→1
```

```
                    TELEMETRY FOR BOX A7

CH #     I CH WEIGHT VOLTAGE    Q CH WEIGHT VOLTAGE

  1            -0.0969                -0.0085
  2            +0.1192                +0.1273
  3            +0.0219                -0.1680
  4            -0.0300                -0.0175
  5            -0.0098                +0.1572
  6            +0.1553                +0.2890
  7            -0.0169                -0.2260
  8            -0.8870                +0.0216

NARROW BAND POWER DETECTOR = 0.0305 volts
WIDE BAND POWER DETECTOR = 0.0057 volts

ATTENUATOR SETTING = 0
METHOD CLOCKED IN = 0 *

* 0=IMMEDIATE, 4=HOP CLOCKED, 8=START OF ADAPTION
12=EITHER HOP CLOCKED OR START OF ADAPTION

DO YOU WANT TO STORE OFFSETS ON TAPE?
Y
```

② →

Refer to Sec. VII for an explanation of the terms. The response (Y) in line 2 indicates the telemetry values are to be stored.

The following is an example of the telemetry program for A13.

TELEMETRY FOR BOX A13

CH #	+1 VOLT REFERENCE	-1 VOLT REFERENCE
1	+1.0040	-1.0130
2	+1.0100	-0.9870
3	+0.9900	-0.9960
4	+0.9850	-1.0030
5	+1.0080	-1.0090
6	+0.9860	-1.0100
7	+0.9910	-0.9960
8	+1.0020	-0.9890

TELEMETRY FOR BOX A13

CH #	PIN DIODE P1	P2	P3	P4
1	-0.5410	-0.4400	-0.4150	-0.7180
2	-0.5800	-0.6200	-0.6980	-0.5200
3	-0.6400	-0.4200	-0.5380	-0.4810
4	-0.7000	-0.4000	-0.7020	-0.6870
5	-0.5800	-0.5300	-0.4980	-0.7230
6	-0.6800	-0.6400	-0.5700	-0.6950
7	-0.0600	-0.6900	-0.4400	-0.4370
8	-0.3600	-0.5000	-0.4700	-0.6260

TELEMETRY PROGRAM
TYPE 1 FOR BOX A7, 2 FOR BOX A13
→2

TELEMETRY FOR BOX A13

CH #	I CH WEIGHT VOLTAGE	Q CH WEIGHT VOLTAGE
1	+0.0301	+0.2660
2	+0.1141	+0.0903
3	-0.0020	-0.1232
4	+0.0640	-0.4880
5	-0.1048	-0.2710
6	+0.1120	+0.3830
7	-0.0649	-0.1329
8	-0.1551	-0.2700

8.1.5 The Telemetry and Command Exercise Test Program

The telemetry and command exercise test program provides for the automatic testing of the controlled units for all possible user entries. All meaningful values are assigned sequentially to the variables so that all possible user entries are checked. No examples are shown as much of the program displays data previously shown and/or in coded format.

8.2 Command and Telemetry

The Telemetry and Control IEEE Bus Interface unit (A1) is the exchange point of data (command, telemetry request, and telemetry) between the Tektronix 4051 Controller and the Weight and Summer Network (A13), the Correlation and Control unit (A7), and the modified Hop Controller. Figures 8.1 and 8.2 show the front panel and internal view of the physical unit while Fig. 8.3 shows a block diagram and the data flow of the unit (A1).

In normal operation, 40 bits of information are composed and formatted in the Tektronix 4051 and transferred via the IEEE bus to the Fairchild 4880 Bus Interface unit in A1 (Ref. 16). The 40 bits (10 4-bit words) are then loaded into a 40 bit buffer in the A1 circuitry where the word is divided into box address, telemetry request, and command. The box address, the four most significant bits, is decoded and controls subsequent data flow by enabling the appropriate hardware. Addresses 0 to 4 are reserved for telemetry while addresses 5 to 9 are reserved for command. The next 16 LSB's form the telemetry request by specifying a particular test point in either A7 or A13. An enable line off the box address decoder is also provided to A7 and A13. Table 8.1 provides a list of test points which can be monitored. The 20 LSb's of the word form the commands to units under A1 control. The decoded box address clocks the commands into latches for delivery to the proper unit. Table 8.2 provides a list of commands which can be issued.

On the input side of A1 is the telemetry associated with the telemetry request. In general, the telemetr, will consist of an I and Q value from the same or different channels of the same unit. The decoded box address

P202-9115

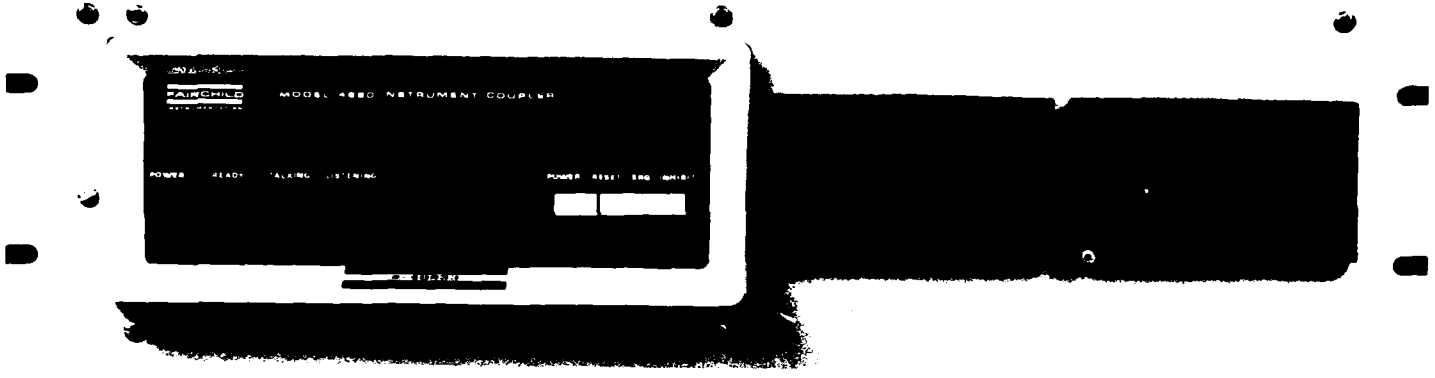


Fig. 8.1. Telemetry and control unit (A1) front panel.

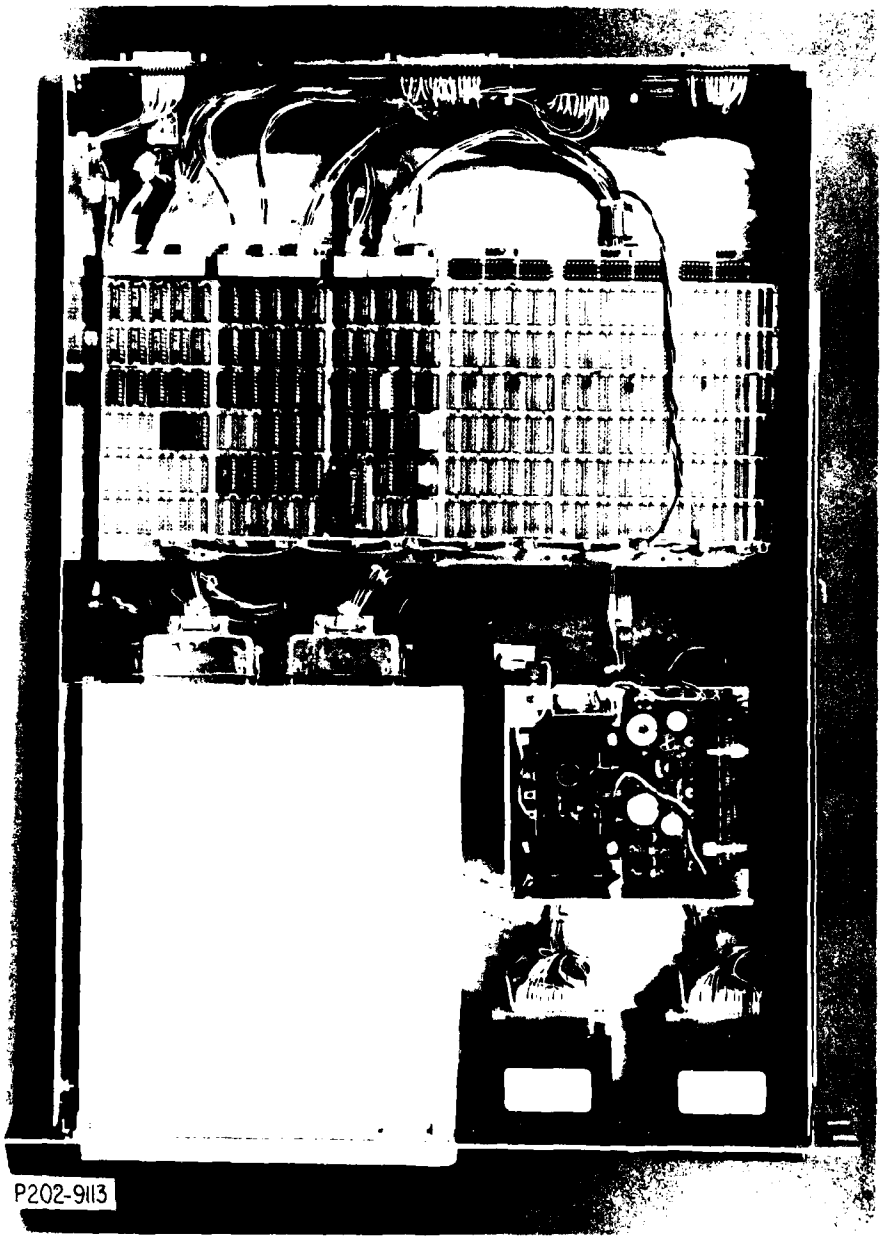


Fig. 8.2. Telemetry and control unit (A1) internal view.

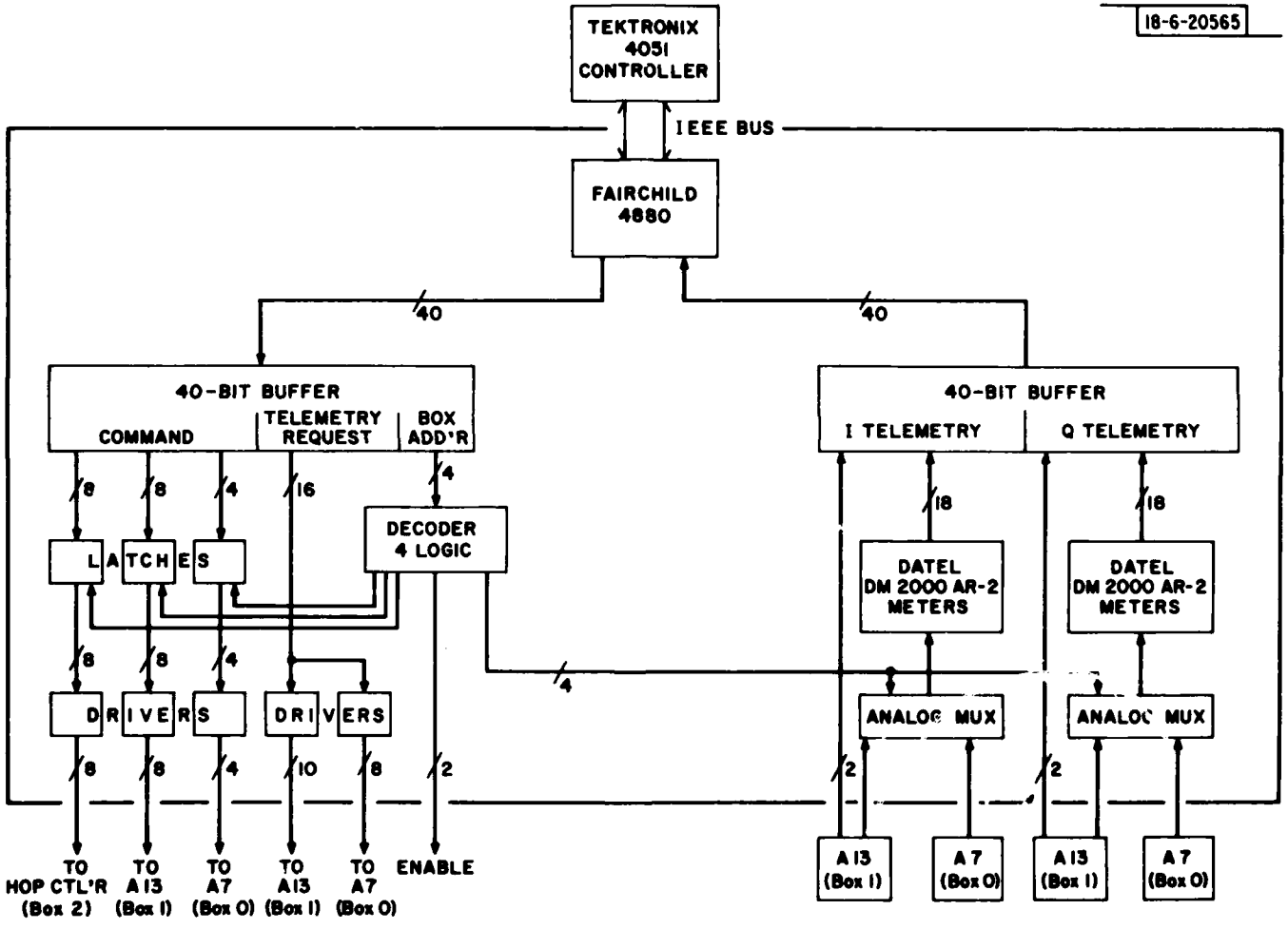


Fig. 8.3. Block diagram telemetry and control unit.

AD-A084 013 MASSACHUSETTS INST OF TECH LEXINGTON LINCOLN LAB F/G 17/4
FEEDBACK NULLING DEMONSTRATION SYSTEM HARDWARE.(U)
NOV 79 D A SIEGEL, D M HODSDON, B M POTTS F19628-80-C-0002
UNCLASSIFIED TN-1979-12 ESD-TR-79-272 NL

2 OF 2

END
DATE FILMED
6-80
DTIC

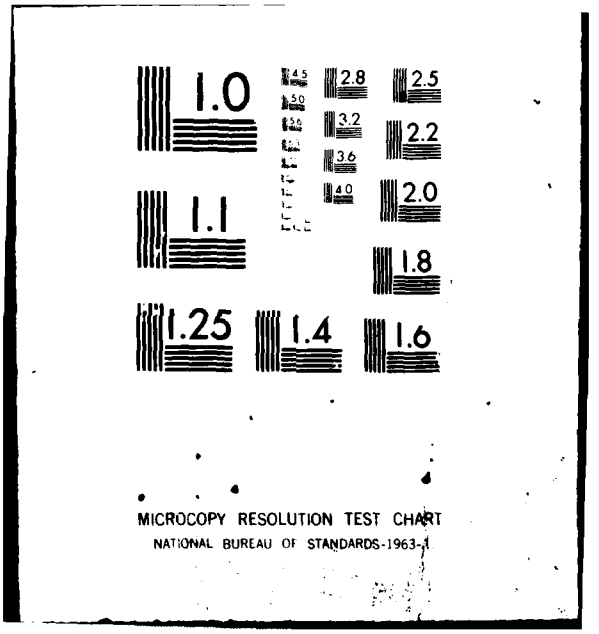

1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

TABLE 8.1

A1 TELEMETRY

	UNIT	BOX #	REQUEST	INFORMATION RETURNED
1.	Correlation & Control (A7)	0	I Channel # Q Channel #	Weight voltages Narrowband power Wideband power
2.	Weight and Summer Network (A13)	1	I Channel # I Test Point # Q Channel # Q Test Point #	Weight voltages PIN Diode voltages Reference voltages
3.	Hop Controller	2	None	----------

TABLE 8.2

A1 COMMANDING

	UNIT	BOX #	COMMAND
1.	Correlation and Control (A7)	5	Set attenuator 0, 5, 10, 15 dB Execute the command 0) immediately 1) at the beginning of the hop pulse edge 2) at the beginning of the adaption edge 3) at the first edge of (1) or (2)
2.	Weight and Summer Network (A13)	6	Combination of transfer switches ON/OFF
3.	Hop Controller	7	Hop control frequency # Hop enable/disable (internal/external hop pulse) Normal/Alternate (hop control frequency # internal/external)

selects one of the analog multiplexer inputs and the information is front panel displayed and A/D converted to a digital format by Datel DM 2000 AR-2 panel meters. The digital output is then clocked into a 40 bit buffer along with some direct digital telemetry, and the information is transferred to the input of the Fairchild 4880 for transfer and display to the Tektronix 4051.

The Telemetry and Control unit was designed with standard TTL logic, Harris 1818A analog multiplexers, and the above mentioned panel meters. Internal to the unit is circuitry for calibrating the panel meters and self testing the unit.

The telemetry request to and telemetry from the Weight and Summer Network (A13) is handled by a specially designed interface card resident in A13. The card consists of Harris 1818A analog multiplexers whose select and enable liner are controlled by A1, whose inputs come from 64 test points within A13 (8 test points for each of 8 channels, 4 I and 4 Q values per channel), and whose outputs return to A1 for display and conversion by the panel meters. Figure 8.4 shows the block diagram for this circuitry. The A13 test points include weight control voltages, PIN diode voltages, and reference voltages (Table 8.1). The interface card also contains the control drivers for the A13 transfer switches (Fig. 8.5) which is an A1 control function (Table 8.2). One of eight or any combination of the eight switches (one per channel) can be turned on or off. The test points and transfer switches are discussed in greater detail in TN 1979-10 on the PIN Diode Weight Circuits (Table 1.1).

8.3 Waveform Analyzer

Biomation Model 1010 waveform rcorders were used to provide high resolution (10-bit A/D conversion) digital waveform capture (4096 words) with amplitude resolution to better than 1/10% and at a conversion rate up to 10 MHz. Numerous record rates are provided, along with versatile control and triggering functions and a digitally adjustable delay (up to 9990 sample intervals). One of the trigger delay/control functions permits triggering before, during, or after the signal has occurred. The "retrigger" allows the recording of the

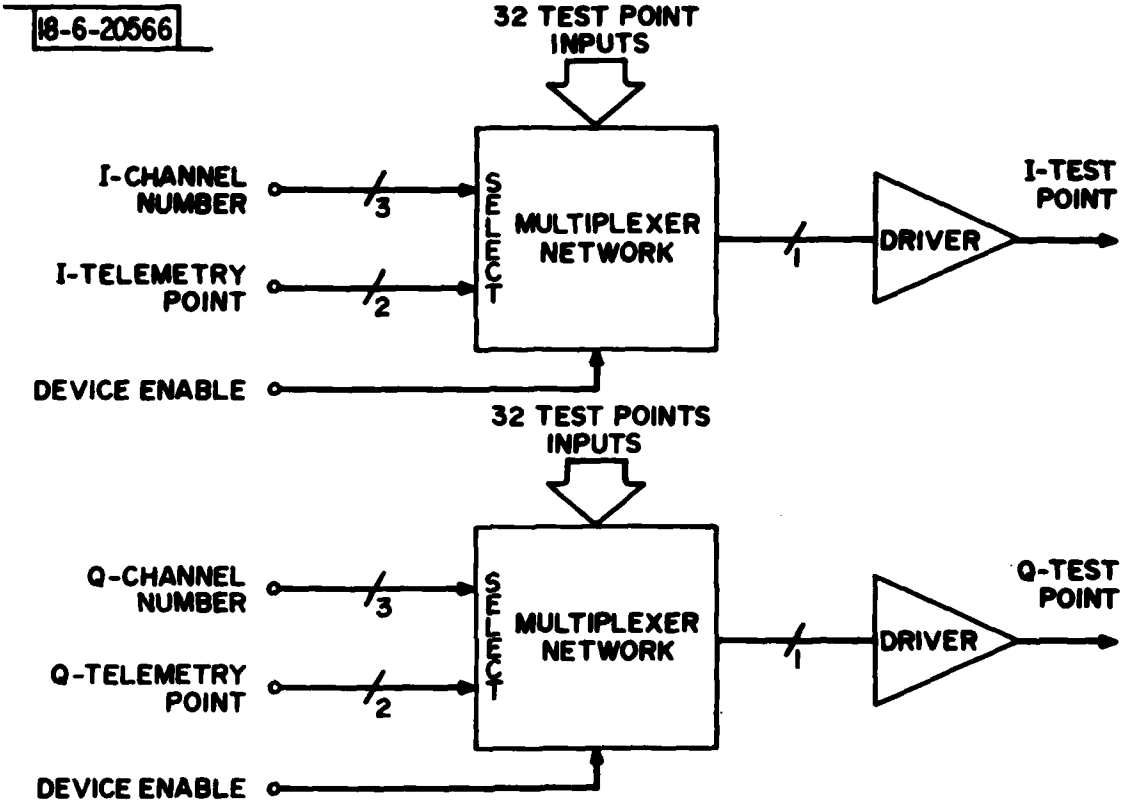


Fig. 8.4. Weight and summer network telemetry card.

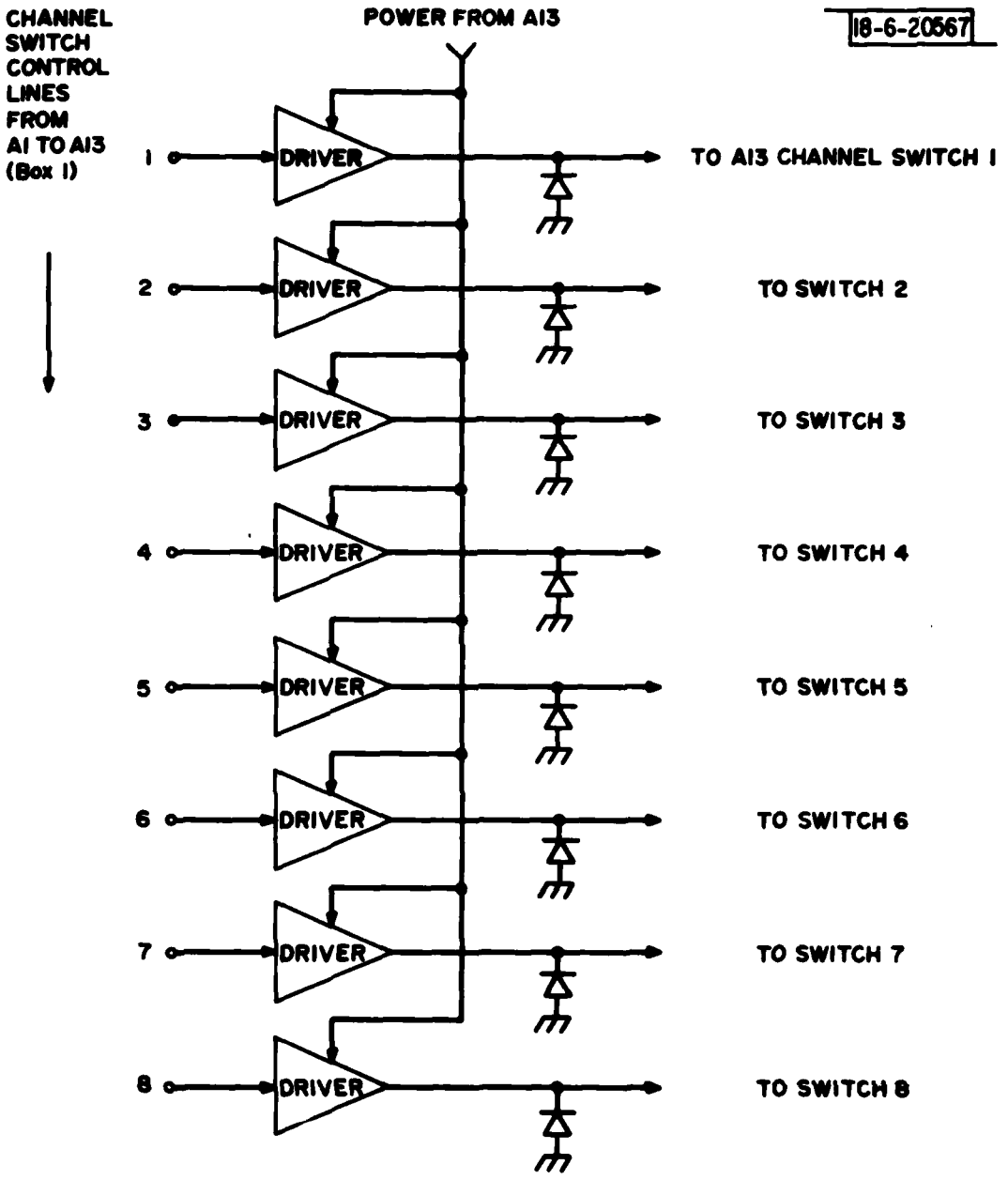


Fig. 8.5. Weight and summer network transfer switch control.

leading baseline of the signal. It is possible for the user to fully record the entire memory or only the first or second half of memory for signal comparison.

There are three types of outputs available on the Biomation 1010. Two analog outputs provide (1) display by an oscilloscope or CRT, and (2) X-Y recorder capabilities. A digital output of the Model 1010 produces 10-bit amplitude data with bit parallel/word serial interface at standard TTL levels. Unfortunately, however, this signal is not compatible with the IEEE BUS which necessitated building a unit to reformat the data in a form usable by the system. A Fairchild Model 4880 Instrument Coupler (Ref. 16) was then used to interface with the IEEE BUS to allow commanding of the waveform recorder by the Tektronix 4051 controller (Sec. 8.1). Figure 8.6 shows a block diagram of the waveform analyzer interfacing to the 4051.

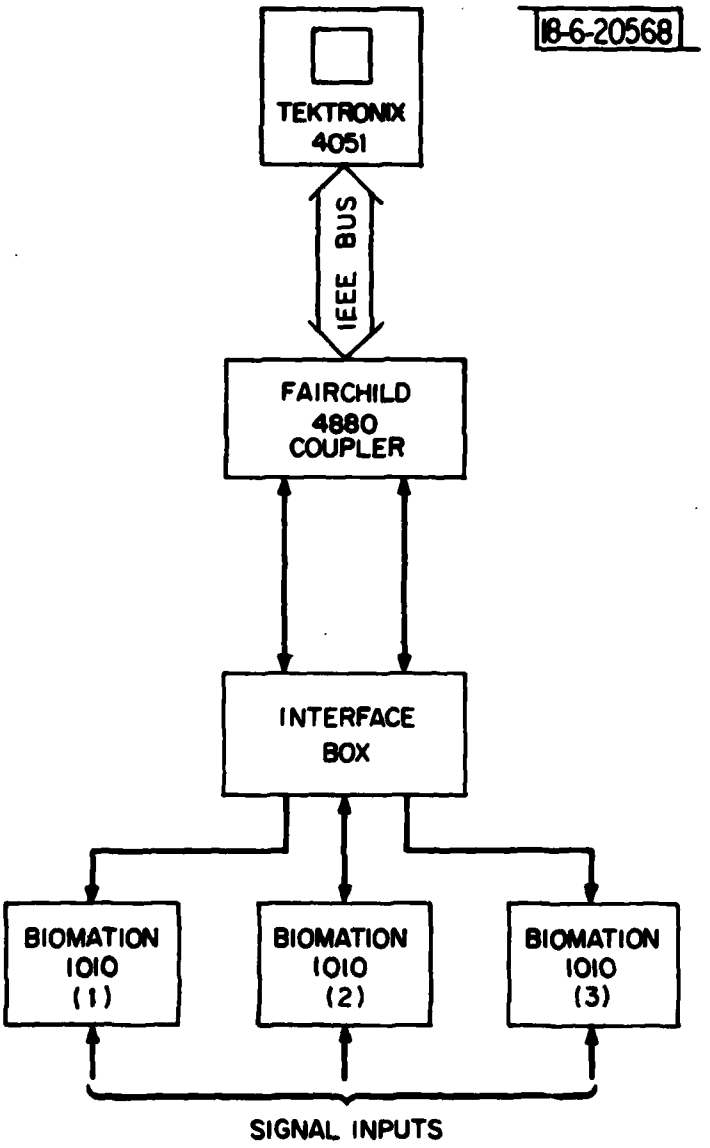


Fig. 8.6. Interface of biomation model 1010 waveform recorder to the adaptive nulling system.

ACKNOWLEDGMENTS

The authors of this report wish to thank the many people who worked so hard in bringing all the complex pieces of this system together and working so well. The knowledge gained from building and testing this system is a tribute to their efforts. In particular, we wish to thank E. Blomberg, D. Brown, T. Emberley, D. Koller, L. Mandeville, F. McCarthy, W. Merritt, D. Newcomb, H. Perras, W. Petersen, R. Sprague, and H. Wolfson.

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GLOSSARY

A/D	Analog-to-digital
AGC	Automatic gain control
ASCII	American standard code for information exchange
BSWS&T	Beam-steering-weight-storage-and-timing unit
BW	Bandwidth
CMD	Command
CRT	Cathode-ray tube
D/A	Digital-to-analog
dB	Decibel
dBmW	Decibel with respect to a 1 milliwatt (10^{-3} watt) reference level
DC	Direct current
DMA	Direct memory access
f_o	Center frequency
FBW	Fractional bandwidth
Freq.	Frequency
GHz	Gigahertz (10^9 Hz)
GPIB	General purpose interface bus
Hz	Hertz (cycles/sec)
I	In-phase
IF	Intermediate frequency
kHz	Kilohertz (10^3 Hertz)
L-band	Frequency band 1 to 2 GHz
LED	Light-emitting diode
LO	Local oscillator
MHz	Megahertz (10^6 Hz)
msec	Millisecond (10^{-3} sec)
PIN	Diode composed of a layer each of positive, intrinsic, and negative material forming junctions.
Q	Quadrature-phase
RAM	Random access memory
RF	Radio frequency
RMS	Root-mean-square
RDM	Read-only memory
S/N	Signal-to-noise ratio
SEC	Second
SPDT	Single-pole-double-throw switch
SYNC	Synchronization
TLM	Telemetry
UHF	Frequency band 225 to 400 MHz
μsec	Microsecond (10^{-6} sec)
V_I	In-phase voltage
V_Q	Quadrature-phase voltage
VDC	Voltage DC
WSN	Weight and summer network

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SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

(19) REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER (18) ESD-TR-79-272	2. GOVT ACCESSION NO. AD-A084 013
	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* (4) Feedback Nulling Demonstration System Hardware	5. TYPE OF REPORT & PERIOD COVERED (9) Technical Note
	6. PERFORMING ORG. REPORT NUMBER Technical Note 1979-12
7. AUTHOR(s) (10) David A. Siegel, David M. Hodsdon, Bing M. Potts, Howard S. Babbitt, Ervin S. Davis, Warren K. Hutchinson, Karen Leeds	8. CONTRACT OR GRANT NUMBER(s) (15) F19628-80-C-0002
9. PERFORMING ORGANIZATION NAME AND ADDRESS Lincoln Laboratory, M.I.T. P.O. Box 73 Lexington, MA 02173	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Program Element No. 63431F Project No. 2029
11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Systems Command, USAF Andrews AFB Washington, DC 20331	12. REPORT DATE (11) 23 Nov[redacted]79
	13. NUMBER OF PAGES 110
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)* Electronic Systems Division Hanscom AFB Bedford, MA 01731 (16) 2.[redacted]7	15. SECURITY CLASS. *(of this report)* Unclassified
	15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)* (12) [redacted]

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

(14) TN-1979-12

18. SUPPLEMENTARY NOTES

None

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

adaptive antenna nulling
analog nulling
signal combining
analog feedback
signal weighting

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The Lincoln Laboratory analog-feedback adaptive antenna nulling demonstration system hardware is described with discussion of design theory, implementation, problems, and trade-offs encountered. System and subsystem block diagrams and photos of actual hardware are included. Peripheral test equipment is discussed along with built-in telemetry and recording capabilities.

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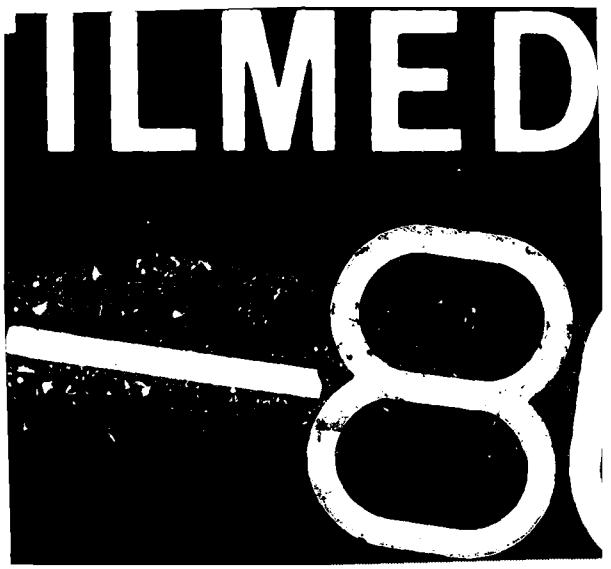
3.07650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